Lab#8 – Lecture 4d

Names: ­­­­­­­­­­­­­­­­\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_, ­­­­­­­­­­­­­­­­\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Date: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Objective:**

This lab #8 is intended to introduce the students to be more comfortable of using the Lab Equipment:

The logic designer, the test equipment, and of course the TTL chips. Most of all you’ll learn more about Design Logic Circuits.

 

**Procedure:**

Use an existing Problem 4-23 on page 225 as show above to perform the following:

1. Use Multisim to draw an XOR logic circuit for a 74LS86 call Figure 1
2. Simulate Figure 1 for each voltage level and record in Table 1.
3. Implement on the breadboard for testing and measuring each voltage level.
4. Record test result in Table 1
5. Repeat step 1-4 using a logic gate NOT, AND, and OR (74LS05, 74LS08 and 74LS32)**\***
6. Record test result for step 5 in Table 2
7. Conclusion
8. **\***

Select two 1kohm resistors.

Reminder: Measure and record the resistance of each resistor.

**Equipment needed:**

1 – Power Supply

1 – Digital Multimeter

2– 1Kohm

1 – 4 position dip switch

1 – 74LS86N - XOR

2– 74LS05N- NOT

2 – 74LS08N- AND

1 – 74LS32N - OR

3 – LED (light Emitted Diode)

Table 1- Lab#8 Schematic

|  |  |  |  |
| --- | --- | --- | --- |
| **Simulated** (Input) | Result | **Test**(Input)  | Result |
| **A** | **B** |  | **A** |  | **B** |  |
| 0 | 0 |  |  |  |  |  |
| 0 | 1 |  |  |  |  |  |
| 1 | 0 |  |  |  |  |  |
| 1 | 1 |  |  |  |  |  |

**Table 1** (Simulation vs Test)

|  |  |  |  |
| --- | --- | --- | --- |
| **Simulated** (Input) | Result | **Test**(Input)  | Result |
| **A** | **B** |  | **A** |  | **B** |  |
| 0 | 0 |  |  |  |  |  |
| 0 | 1 |  |  |  |  |  |
| 1 | 0 |  |  |  |  |  |
| 1 | 1 |  |  |  |  |  |

**Table 2 XNOR** (Simulation vs Test)

Observations:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_