Lab 9 – 1 to 3 clock using JK Flip Flops and 555 Timer

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The purpose of this lab is to:

Many times you can use multiple harmonically related clocks to test a combinational circuits. The Purpose of this lab is to show students how to create a small multiple clock counter circuit that uses JK Flip Flops and a 55 Time

Equipment needed:

1 – 555 Timer

1 – 1Kohm

1 – 4 position dip switch

2 – 74LS73 Dual JK flip flop with clear

2 – Resistors (To Be Designed)

2 – Capacitors (To Be Designed)

Using Multisim simulate design and build a very low frequency clock using a 555 Timer, two resistors and two capacitors. To do this you will need to use the datasheet, Excel and Multisim. Record the component and performance values in Table 1



Figure 1 - Lab 9 Astable Oscillator (Clock)

|  |  |  |
| --- | --- | --- |
|  | Designed | Measured |
| RA = | 4.7kΩ | 4.6307kΩ |
| RB = | 100kΩ | 100.33kΩ |
| C = | 1µF | 1.014µF |
| t1 = | 72.557ms | 70ms |
| t2 = | 69.300ms | 73ms |
| T = | 141.857ms | 143.6ms |
| f = | 7.035Hz | 6.964Hz |
| f = | 7.049Hz | n/a |
| D = | 0.489 | 0.4895 |

Table 1 Simulation vs Test



Figure 2 – 3 bit counter using 74LS73s

Verify that there are 3 unique clocks that are harmonically related to CLK1

Observations:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_