Worst Case Analysis of Electronics Using Parameter Design Techniques

by

Mr. Andrew G. Bell & Mrs. Catherine M. Vincent

ITT Industries A/CD
Fort Wayne, Indiana

Worst Case Analysis of Electronics Using Parameter Design Techniques

- Introduction
  - ITT Aerospace/Communications (A/CD) has facilities in Fort Wayne, Indiana and Clifton, New Jersey that employees 1,976 people.
  - This presentation is based on a “Parameter Design Technique” used on a space project power supply worse case analysis within the Fort Wayne headquarters.

ITT Industries
Engineered for life

Worst Case Analysis of Electronics Using Parameter Design Techniques

- Introduction
  - ITT A/CD products include the U.S. Army SINCGARS and U.K. BOWMAN tactical communication system, voice data switches, data entry terminals, fiber optics transmission systems, ground to air radios used by the Federal Aviation Administration (FAA), and a family of secure communications terminals: space-based navigation and atmospheric remote sensing payloads—GPS, Alpha, GOES Imager/Sounder, AVHRR and HIRS Instruments.

Worst Case Analysis of Electronics Using Parameter Design Techniques

- Background

Classical Worst Case Analysis has been used to demonstrate electronic design "robustness" over the years on numerous space and communication programs at ITT A/CD. The amount of time (computer time and set up time) it takes to complete a WCA can vary greatly based upon the complexity of the design and performance being measured. This variance can be compounded by a simulation failure requiring engineering intervention or the need to execute multi-run simulations.

An alternate "Parameter Design Technique" approach which requires fewer simulations has been successfully used at ITT A/CD to demonstrate a similar quality measurement in far less time.

Worst Case Analysis of Electronics Using Parameter Design Techniques

- Objectives

  Compare the Classical Worst Case Analysis approach to the alternate "Parameter Design Technique" by analysis of the maximum group delay of a 4 pole transitional Butterworth-Thompson lowpass filter. All simulations were performed on an UltraSPARC-II 400MHz Sun UNIX Workstation.

- If a circuit's "robustness" can be demonstrated using a technique that produces similar quality measurement relative to the classical techniques there could be:
  - from an engineering standpoint - significant time savings.
  - from a customer standpoint - a cost savings
  - from a managerial standpoint - similar design risk in less time and money.

Worst Case Analysis of Electronics Using Parameter Design Techniques

- Approach
  - Using Analog Workbench build a circuit simulation model for a simple 4 pole transitional Butterworth-Thompson lowpass filter.
  - Using classical worst case analysis techniques, predict the circuit's worst case group delay performance and measure the simulation time.
  - Use a "Parameter Design Technique" to predict the circuit's worst case performance.
    - Select important noise factors
    - Select appropriate orthogonal array and run experiments
    - Evaluate the simulation results using an analysis of means
    - Determine appropriate confirmation run
  - Compare "Parameter Design Technique" results to the classical approach.

Worst Case Analysis of Electronics Using Parameter Design Techniques

- Classical Approach

Components are assigned Gaussian distributions for variation.

User Variables: BASELINE CIRCUIT

VCC=15
VSS=-15

A C1=4000E-12, 5%, 5%, GAUSS0.4
C2=147E-12, 5%, 5%, GAUSS0.4

B R1=5E3, 1%, 1%, GAUSS0.4
R2=5E3, 1%, 1%, GAUSS0.4

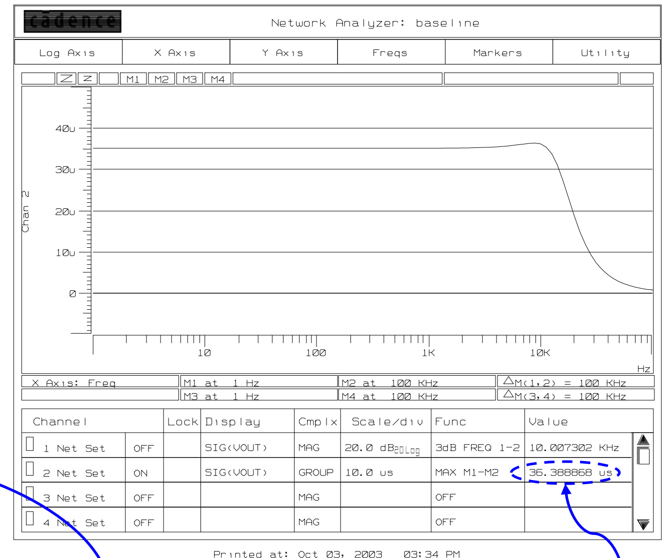
C R3=40E3, 1%, 1%, GAUSS0.4

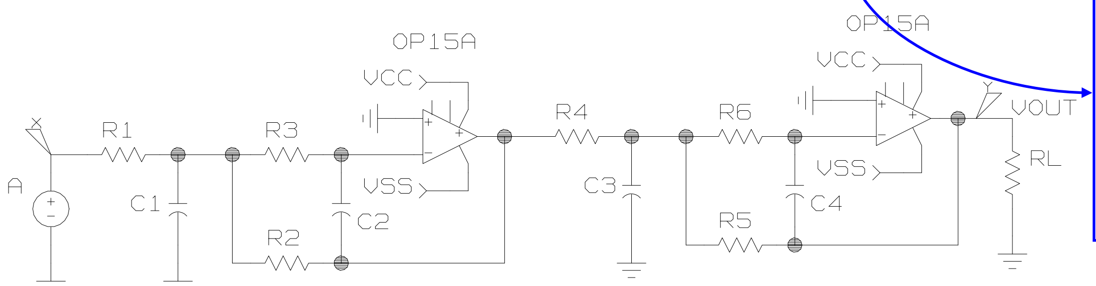
D C3=2650E-12, 5%, 5%, GAUSS0.4
C4=265E-12, 5%, 5%, GAUSS0.4

E R4=5E3, 1%, 1%, GAUSS0.4
R5=5E3, 1%, 1%, GAUSS0.4

F R6=40E3, 1%, 1%, GAUSS0.4

G RL=50E3, 5%, 5%, GAUSS0.4





Tolerance all components and run an EVA Sensitivity/Worst Case and Monte Carlo Analyzes that measure the variation in group delay

Worst Case Analysis of Electronics Using Parameter Design Techniques

- Alternate Approach
  "Parameter Design Technique"
  - Select important noise factors
    - brainstorm with others on what is important
    - group terms if possible

Noise Factors	A	B	C	D	E	F	G
1	C1 & C2 (min)	R1 & R2 (min)	R3 (min)	C3 & C4 (min)	R4 & R5 (min)	R6 (min)	RL (min)
2	C1 & C2 (max)	R1 & R2 (max)	R3 (max)	C3 & C4 (max)	R4 & R5 (max)	R6 (max)	RL (max)

  - Select appropriate orthogonal array

Simulations	Run	A	B	C	D	E	F	G
ortho1	1	1	1	1	1	1	1	1
ortho2	2	1	1	1	2	2	2	2
ortho3	3	1	2	2	1	1	2	2
ortho4	4	1	2	2	2	2	1	1
ortho5	5	2	1	2	1	2	1	2
ortho6	6	2	1	2	2	1	2	1
ortho7	7	2	2	1	1	2	2	1
ortho8	8	2	2	1	2	1	1	2

In our case, we selected component groupings based upon knowledge of the circuit's operation. This reduced the number of noise factors down to six. Then we added the load resistance.

The L8 Orthogonal Array was selected. It allows for us to test two values for each noise factor. In our example, we selected minimum and maximum values of the factors to be equal to the minimum and maximum values of the components based upon the tolerance of each part.

ITT Industries
Engineered for life

Worst Case Analysis of Electronics Using Parameter Design Techniques

- Alternate Approach
  "Parameter Design Technique"

User Variables: ORTHO1 CIRCUIT

VCC=15
VSS=-15

A C1=4000E-12*0.95
C2=147E-12*0.95

B R1=5E3*0.99
R2=5E3*0.99

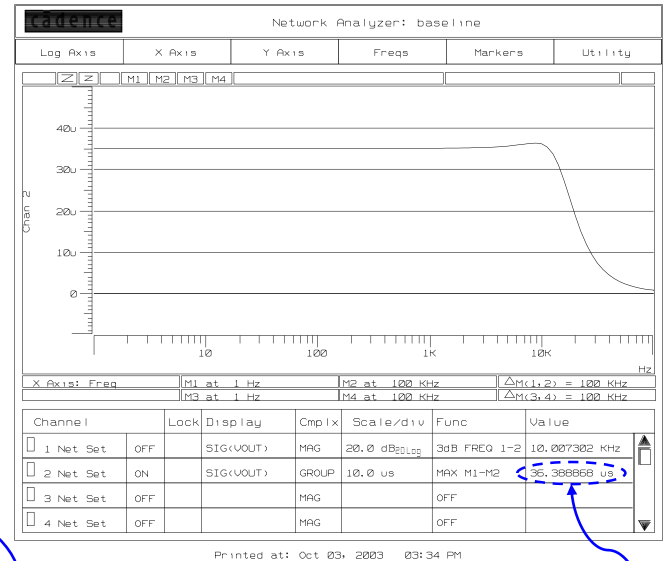
C R3=40E3*0.99

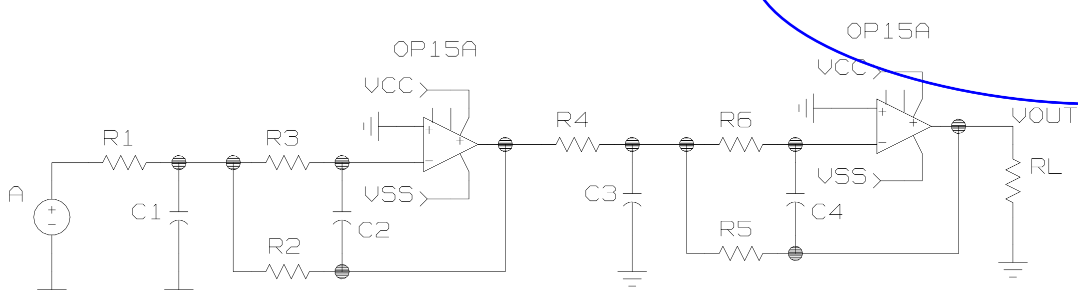
D C3=2650E-12*0.95
C4=265E-12*0.95

E R4=5E3*0.99
R5=5E3*0.99

F R6=40E3*0.99

G RL=50E3*0.95





Built and ran eight simulation circuits that measured the group delay.

ITT Industries
Engineered for life

Worst Case Analysis of Electronics Using Parameter Design Techniques

- Results

  "Parameter Design Technique"

Simulations	Run	A	B	C	D	E	F	G	Results (usec)
ortho1	1	1	1	1	1	1	1	1	34.22
ortho2	2	1	1	1	2	2	2	2	35.75
ortho3	3	1	2	2	1	1	2	2	34.75
ortho4	4	1	2	2	2	2	1	1	35.79
ortho5	5	2	1	2	1	2	1	2	37.43
ortho6	6	2	1	2	2	1	2	1	38.09
ortho7	7	2	2	1	1	2	2	1	37.51
ortho8	8	2	2	1	2	1	1	2	38.13

The raw data for the eight runs was collected and placed into a table. The results show that the group delay of the filter varied between 38.13 μsec and 34.22 μsec.

Total simulation time was 8 seconds.

Worst Case Analysis of Electronics Using Parameter Design Techniques

- Analysis - Using the Analysis of Means "Parameter Design Technique"

Simulations	Run	A	B	C	D	E	F	G	Results (usec)
ortho1	1	1	1	1	1	1	1	1	34.22
ortho2	2	1	1	1	2	2	2	2	35.75
ortho3	3	1	2	2	1	1	2	2	34.75
ortho4	4	1	2	2	2	2	1	1	35.79
ortho5	5	2	1	2	1	2	1	2	37.43
ortho6	6	2	1	2	2	1	2	1	38.09
ortho7	7	2	2	1	1	2	2	1	37.51
ortho8	8	2	2	1	2	1	1	2	38.13

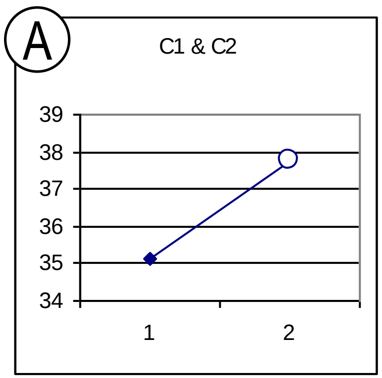
confirmation	9	2	2	2	2	2	2	2

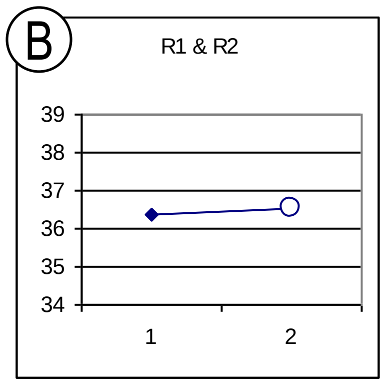
	AVE (1)	AVE (2)
A	3.51E+01	3.78E+01
B	3.64E+01	3.65E+01
C	3.64E+01	3.65E+01
D	3.60E+01	3.69E+01
E	3.63E+01	3.66E+01
F	3.64E+01	3.65E+01
G	3.64E+01	3.65E+01

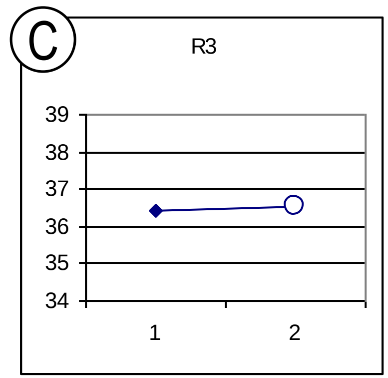
An Analysis of Means (ANOM) is performed on the results to determine which confirmation run might produce the greatest amount of group delay.

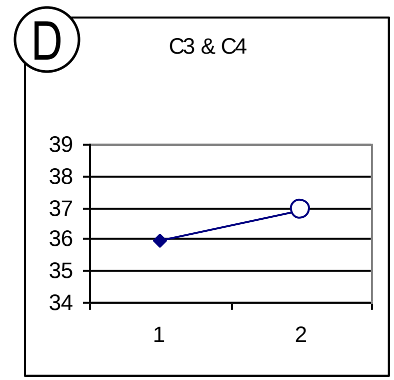
Worst Case Analysis of Electronics Using Parameter Design Techniques

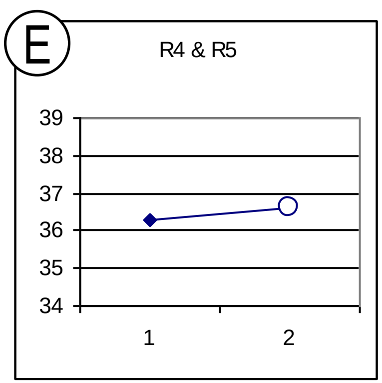
- Analysis - Factor Plots "Parameter Design Technique"

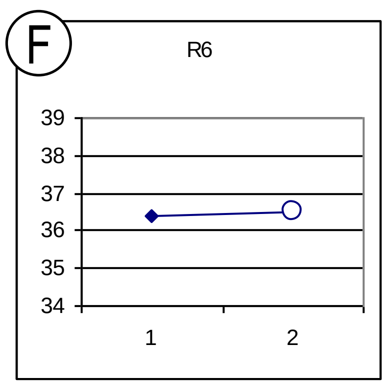


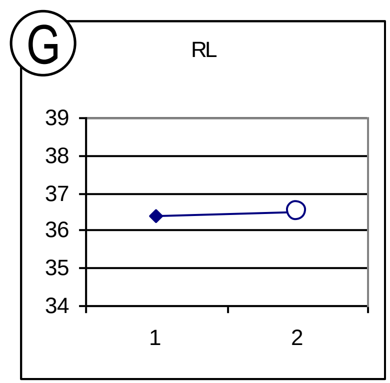








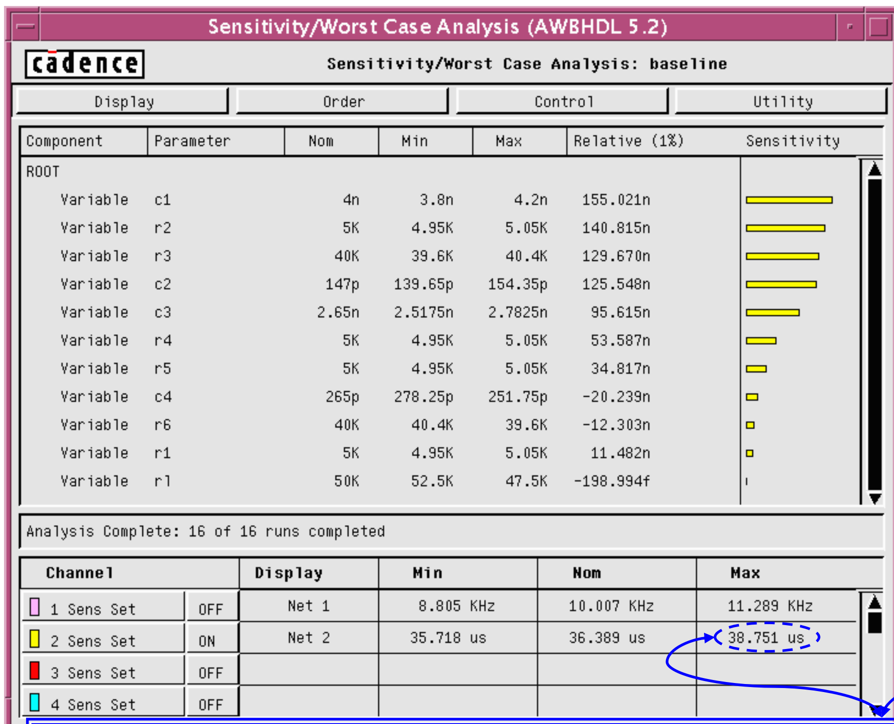




In this case, the proposed confirmation run that produces the greatest group delay is when all noise factors are at their maximum.

Worst Case Analysis of Electronics Using Parameter Design Techniques

- **Analysis** - using Classical Worst Case Analysis



Sensitivity/Worst Case Analysis (AWBHDL 5.2)

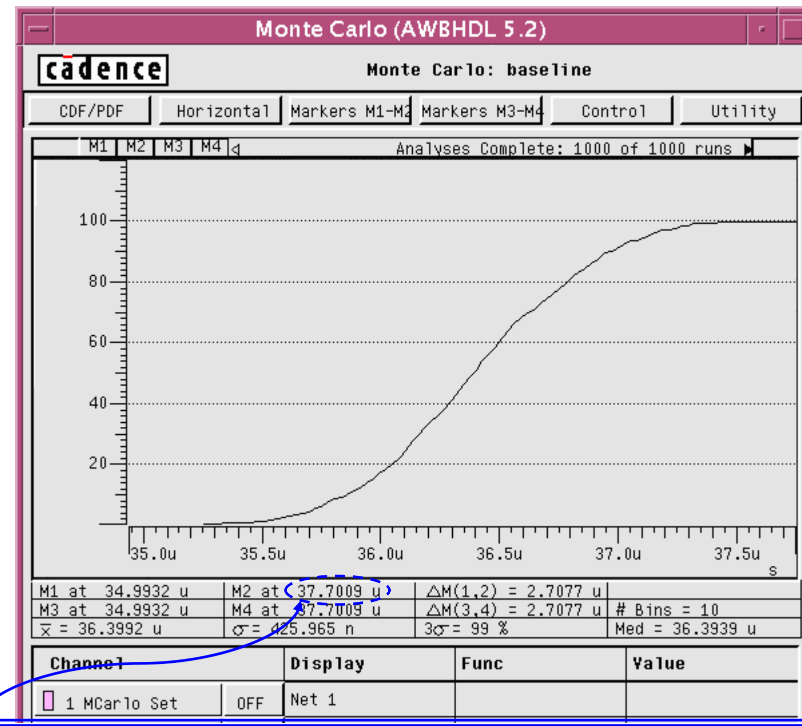
cadence — Sensitivity/Worst Case Analysis: baseline

Display | Order | Control | Utility

Component	Parameter	Nom	Min	Max	Relative (1%)
ROOT					
Variable	c1	4n	3.8n	4.2n	155.021n
Variable	r2	5K	4.95K	5.05K	140.815n
Variable	r3	40K	39.6K	40.4K	129.670n
Variable	c2	147p	139.65p	154.35p	125.548n
Variable	c3	2.65n	2.5175n	2.7825n	95.615n
Variable	r4	5K	4.95K	5.05K	53.587n
Variable	r5	5K	4.95K	5.05K	34.817n
Variable	c4	265p	278.25p	251.75p	-20.239n
Variable	r6	40K	40.4K	39.6K	-12.303n
Variable	r1	5K	4.95K	5.05K	11.482n
Variable	r1	50K	52.5K	47.5K	-198.994f

Analysis Complete: 16 of 16 runs completed

Channel		Display	Min	Nom	Max
1 Sens Set	OFF	Net 1	8.805 KHz	10.007 KHz	11.289 KHz
2 Sens Set	ON	Net 2	35.718 us	36.389 us	38.751 us
3 Sens Set	OFF				
4 Sens Set	OFF				

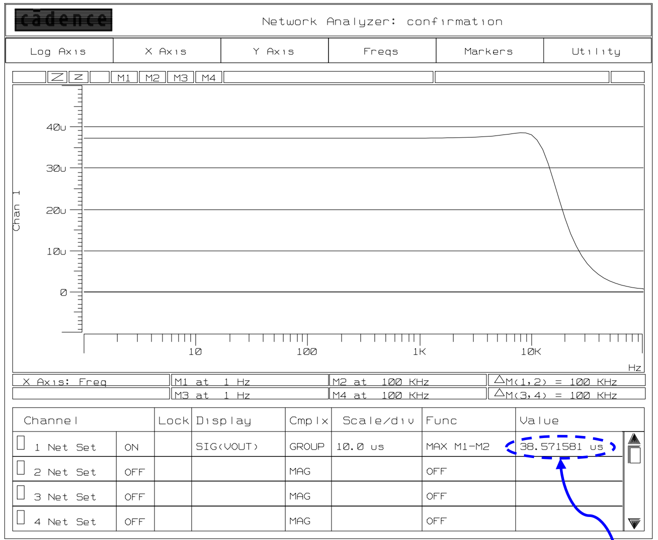


EVA Sensitivity/Worst Case result of 38.75 μsec required 16 seconds of total simulation time.

Monte Carlo worst case result of 37.7 μsec required 16 minutes and 40 seconds total simulation time.

Worst Case Analysis of Electronics Using Parameter Design Techniques

- Confirmation



⊕ User Variables: CONFIRMATION CIRCUIT

VCC=15
VSS=-15

A C1=4000E-12*1.05
C2=147E-12*1.05

B R1=5E3*1.01
R2=5E3*1.01

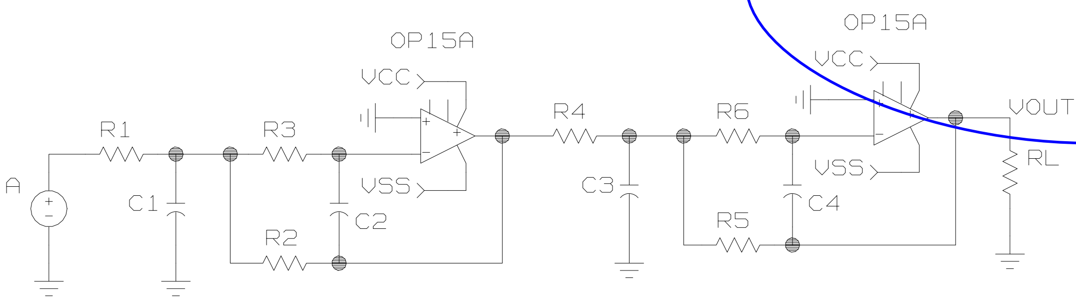
C R3=40E3*1.01

D C3=2650E-12*1.05
C4=265E-12*1.05

E R4=5E3*1.01
R5=5E3*1.01

F R6=40E3*1.01

G RL=50E3*1.05



With the factors changed for the confirmation run the predicted worst case group delay is about 38.57 μsec.

Total simulation time was 1 second.

ITT Industries
Engineered for life

Worst Case Analysis of Electronics Using Parameter Design Techniques

- Conclusions

Simulations	Run	A	B	C	D	E	F	G	Results (usec)
ortho1	1	1	1	1	1	1	1	1	34.22
ortho2	2	1	1	1	2	2	2	2	35.75
ortho3	3	1	2	2	1	1	2	2	34.75
ortho4	4	1	2	2	2	2	1	1	35.79
ortho5	5	2	1	2	1	2	1	2	37.43
ortho6	6	2	1	2	2	1	2	1	38.09
ortho7	7	2	2	1	1	2	2	1	37.51
ortho8	8	2	2	1	2	1	1	2	38.13
confirmation	9	2	2	2	2	2	2	2	**38.57**
Monte Carlo									**37.70**
EVA									**38.75**

In this example, the alternate "Parameter Design Technique" produced a worst case result that was greater than the 1000 run Monte Carlo but less than EVA.

This is not to suggest that we abandon the classical approaches because sometimes they will produce results that are more accepted by our customers and may show "true" worst case performance. However, in some cases an alternate approach may be acceptable to the customer and more cost effective.

<u>Total simulation times</u>

Parameter Design Technique = 9 sec
EVA Sensitivity/Worst Case = 16 sec
Monte Carlo = 16 min and 40 sec

Worst Case Analysis of Electronics Using Parameter Design Techniques

- Acknowledgements

We would like to thank Eric Smith and George Adamczyk for allowing us to write this paper.