EMA Currents

An Informative e-Newsletter from EMA Design Automation

Newsletter

Special Offer
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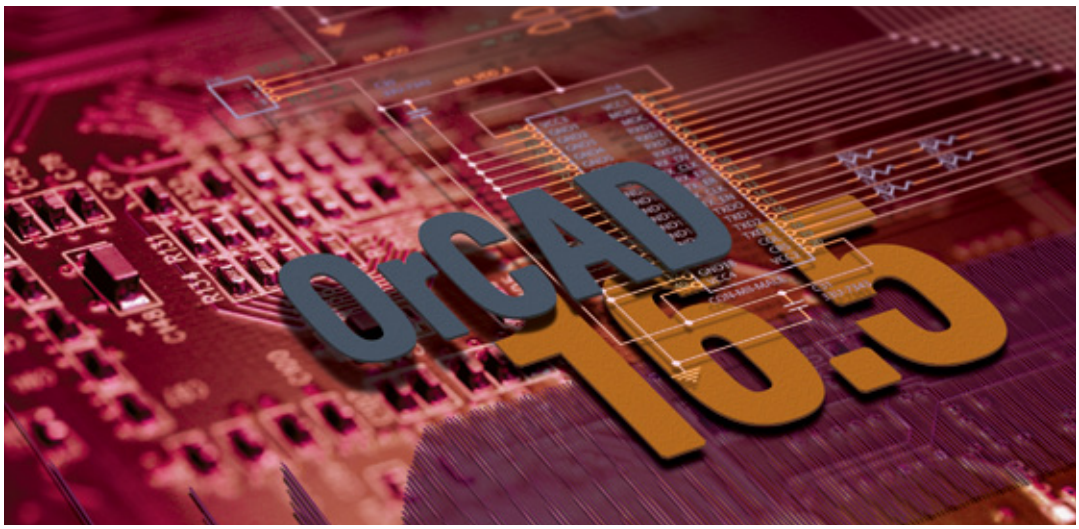
Cadence Unveils the OrCAD Capture Marketplace

The evolution of the Internet and online design content has forever altered the way engineers access information. Utilization of online design content is no longer a preference but an integral part of the design process. To meet this need Cadence is launching an industry-first online PCB reference library and app store.

Continued on page 11 >

Also in this issue:



What's New in Cadence OrCAD 16.5

New Suites, Advanced PCB Editing, Integrated Signal Integrity Analysis and More

Earlier this year Cadence® released the highly anticipated OrCAD® version 16.5, and while many customers have quickly upgraded to take advantage of the new capabilities in this release, some still have not made the move to OrCAD 16.5. Read on for a brief overview of what's new in OrCAD 16.5 and why you should take notice! Based on Cadence Allegro® technology, release 16.5 addresses the need for an affordable PCB tool that meets the increasing design requirements, complexity, and constraints of today's products. Tools once reserved for the largest corporations are now affordable for mainstream designers.

The highlights of Version 16.5 include key added features, especially in the PCB Editor. These tools, further discussed on page 2, include differential pair routing, circuit replication, improved simulation capabilities and more. Cadence has also restructured the OrCAD design suites to create products that better fit today's designers. These new suites have reconfigured OrCAD into three separate offerings; users of all levels can find the right software to meet their specific design needs. With these packages OrCAD provides the greatest mix of functionality/cost in the industry.

Introducing New Suites

OrCAD PCB Designer Lite is a free limited version of OrCAD that allows users to evaluate the software and view designs. It can even be used for design work that falls within certain size and part limits. It helps introduce all the features and functionality of OrCAD, allowing users to seamlessly transition to the full-featured tools with which it's fully compatible.

OrCAD PCB Designer Standard contains all the main tools necessary for PCB Design in an economical package. It includes schematic entry, PCB editing, manufacturing outputs, and 3D visualization. Standard is the ideal tool for many designers, with optional upgrades for scalability.

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EMA Design Automation™
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You are invited: OrCAD PCB Editor 16.5 Virtual Seminar

In case you missed the OrCAD 16.5 Seminar you can still get all the details in the virtual seminar. We will introduce you to what's new and exciting in the latest release of Cadence OrCAD PCB Editor. The focus of this seminar is board layout and routing. It will demonstrate the enhancements made in version 16.5 and offer helpful tips and tricks you can use in PCB Editor.

Seminar attendees will learn:

- New features in release 16.5 such as differential pair support, region based routing rules, placement replication, Intelilgent PDF generation, and much more....
- How to increase productivity and efficiency during the board layout process
- How PCB Editor can optimize your designs for performance, yield, cost, and reliability
- Solutions and explanations to common user questions

Watch this seminar at www.ema-eda.com/seminar

Continued from front cover

	OrCAD EE Designer	OrCAD PCB Designer Professional	OrCAD PCB Designer Standard	OrCAD PCB Designer Lite
Schematic Entry	●	●	●	Limited
Analog Mixed Signal Simulation	●	Option		Limited
Advanced Analysis	Option	Option		Limited
PCB Editing		●	●	Limited
Differential Pair Support		●		Limited
Advanced Rules and Constraints		●		Limited
Manufacturing Outputs		●	●	Limited
3D Visualization		●	●	Limited
Basic Signal Integrity Analysis		●		
Autorouting		●		Limited
256 Layer Autorouting		Option		
Component Data Management	Option	Option	Option	Limited
FPGA PCB Co-design	Option	Option	Option	
Full Signal Integrity Analysis	Option	Option	Option	

OrCAD PCB Designer Professional suite includes additional functionality in the areas of constraint management, advanced PCB editing, placement upgrades, and signal integrity analysis. These capabilities, typically found on significantly higher cost software, contain many automated features that are essential for completing complex designs in realistic time-frames. We see eliminating manual error-prone processes as key to allowing designers to work at both a high-level of efficiency and creativity.

Advanced PCB Editing Features

A major area of improvement for version 16.5 is the PCB Editor. Differential pair support has been added with features such interactive and automatic routing as well as support for diff pair specific constraint generation and design rules checking (DRC). 16.5 upgraded the integrated constraint manager to define electrical rules like min/max length, region rules, and even layer specific design rules; all of which are dynamically checked in real-time as you route. Some major time saving features are PCB placement replication for reusing placement across channels, an automated TestPrep function for efficient testpoint generation, and associative dimensioning to automatically update dimensions as objects are moved. OrCAD 16.5 provides a full set of PCB editing tools to manage and define design intent from logical schematic through physical implementation.

Enhanced Schematic Editing Features

Additional features and enhancements have been made to OrCAD Capture. The new release introduces the concept of NetGroup, which can create groups of nets. The new NetGroup Connector can be used to intelligently merge and tap out signals and to generate net names for connected signals. Some nice touches have also been made to the Intelligent PDF Generation Utility; including live off page connector links in the PDF and the ability to open referenced PDF files defined in the schematic properties such as component datasheets. These tools greatly boost the value of sending a PDF by ensuring it includes complete information and is easily searchable.

Integrated Simulation & Analysis

Full Signal Integrity analysis is a requirement to ensure compliance with many of the high speed standard interfaces in use today. OrCAD PCB SI provides a fully integrated pre and post layout signal integrity analysis environment, but what really makes it stand out is direct integration into the OrCAD PCB Editor constraint manager. This integration into the PCB design flow allows you to generate design constraints directly from your simulation results, an ability not offered by other PCB tools. Additionally 16.5 introduced partial design simulation for PSpice that unifies the PCB and simulation flow by enabling the designer to use a single schematic for both simulation and PCB implementation. Using it you can simulate specific circuits in the design with different simulation profiles to create greater design efficiency.

Support

Many users will be happy to know that this release is fully supported on Windows 7, 32 and 64 bit systems, including support for Windows UAC.

Contact Us

To get the latest version of OrCAD or learn more about how 16.5 can work for you, contact EMA sales at info@ema-eda.com. If you are currenly and on-maintenence OrCAD user and want to upgrade to 16.5, visit support.ema-eda.com Also, check out our article on the new Cadence OrCAD Marketplace, page 11, another way 16.5 is changing PCB design.

Is Phase Margin Enough to Prove Stability?

By Andrew G. Bell, Senior Staff Engineer, ITT Geospatial Systems

Classically, the small signal stability of a circuit has been evaluated by measuring its open loop Phase Margin. Phase Margin is equal to the 180° minus the phase shift measured at the circuit's open loop cross-over frequency (0 dB point). Many years ago a colleague of mine asked me why his LED driver circuit (shown in Figure 1) was oscillating in the lab when his Cadence PSpice® stability analysis showed that he had 30 degrees of Phase Margin (shown in Figure 2). Upon further investigation, we discovered that he had not accounted for the impact of the DC operating point in the AC small signal analysis.

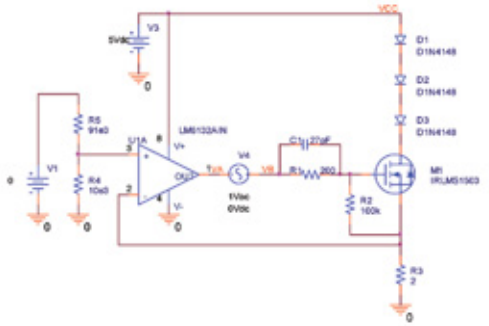


Figure 1 Initial Simulation Circuit

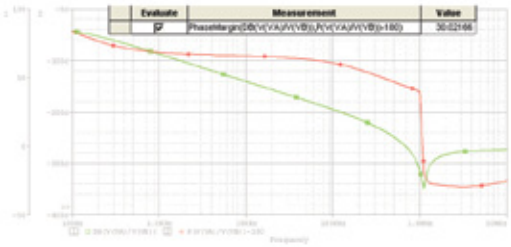


Figure 2 Initial Open-Loop Response

To evaluate why the Phase Margin did not predict the instability of the circuit, the load on the op amp is reviewed. With V1 set to zero volts, the load impedance is measured and at 10 kHz the capacitive load is only 360pF. This should not have been a problem with the LM6132 op amp stability.

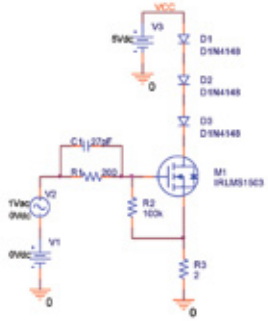


Figure 3 Test Circuit for Impedance Measurement

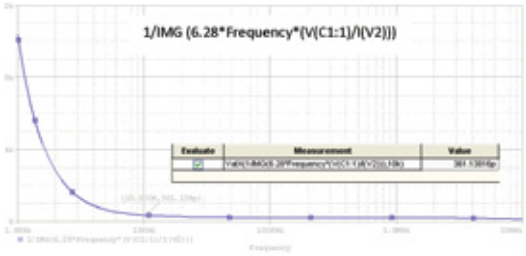


Figure 4 Impedance Measurement

Both of the simulations above are small signal AC simulations that assume that the circuit is linear and operates around a fixed DC operating point. Is this a valid assumption for the circuit? Maybe this would be an acceptable assumption if the load were fixed, but in this case the MOSFET will transition from an "off" to "on" state when the Vgs voltage is changed from zero to five volts.

In Figure 4, load impedance is being measured, in particular the capacitance. As you know,

Xc =1/2∏fc or C = 1/2∏fXc or C = 1/2∏f*img(V/I)

can be plotted using the PSPICE measurement

1/IMG(6.28*Frequency*(V(C1:1)/I(V2))).

Also as a test, consider the measurement of a 300pF capacitor using the approach defined above. The measurement shows that the capacitance is indeed 300pF.

Next, we will resimulate the circuit with the MOSFET turned "on." This time the phase margin reduces to only 2.1 degrees. Would this explain the instability seen in the lab? Why did the stability change when the MOSFET turned "on"?

In the schematic (Figure 5) a 5V source is tied to the Anode of the LED and the MOSFET source is tied to 2 ohm and inverted input to the op amp. With the input voltage at zero, the MOSFET is turned "off" (not really, the MOSFET is on but there is a very small current draw, 1.5mA) and Vgs = 2.64V. But when the input voltage is switched to 5V the MOSFET turns "on," the current draw jumps to 250mA and Vgs = 2.92V. If you are thinking that there is some sort of VDS bias problem please refer to the Output Characteristic curve below.

Continued on page 4 >

OrCAD ISR S007: How and Why to Stay Current

Cadence provides OrCAD Interim Software Releases twice a month. These releases not only improve software stability but include additional features that have been requested by users. On maintenance users should be sure they are updating their software to provide the best possible experience.

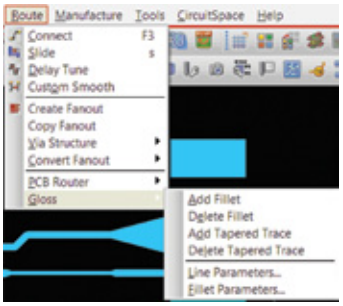
Where to get ISR's

EMA users can download their updates directly from the EMA start page in OrCAD Capture.

Included in Release S007

S007 saw the addition of two key features, Fillets and Tapered Traces. These tools were previously only available to Allegro users, but can now be found in the OrCAD Professional Suite.

A common use for fillets is in flex circuits where the added strength of the fillet is necessary. Tapered Traces perform a similar strength adding role along a trace with changes in width. These new features can be found under Route>Gloss.



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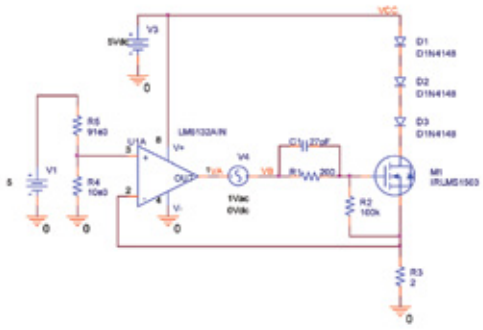


Figure 5 Simulation with MOSFET biased "on"

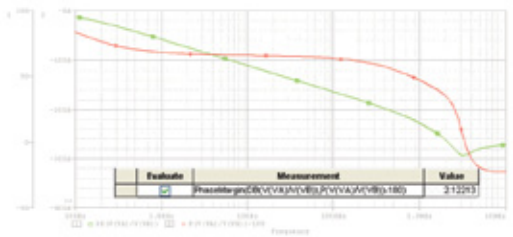


Figure 6 Open-Loop Response with MOSFET biased "on"

The Total Gate Charge (shown in Figure 7) for the IRLMS1503 MOSFET is about 4nC for a Vgs voltage of 5V. This would translate into a capacitive load of C = 800pF.

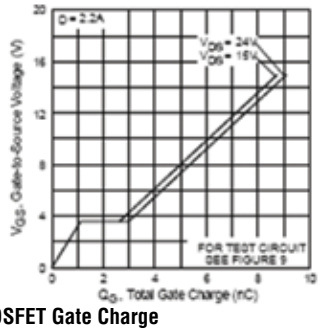


Figure 7 MOSFET Gate Charge

This could introduce instability and cause the LED driver to oscillate. This is a roundabout way of saying that because bias was not included in the original analysis, a transient analysis could provide more information relative to the circuit's stability. Of course, a 2.1 degree phase margin would have also shown that the circuit was unstable.

In a transient analysis (shown in Figure 8) the MOSFET turns "on" and "off" and shows significant ringing and overshoot in response to an input pulse (transient response shown in Figure 9). The instability is clearly present in the transient response.

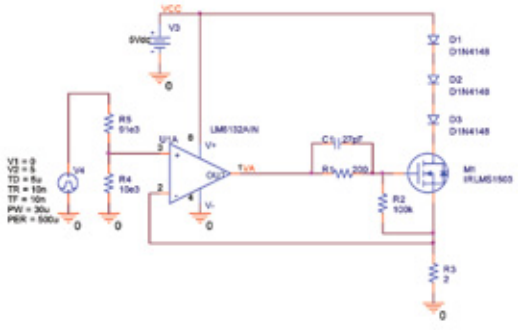


Figure 8 Transient Simulation Circuit

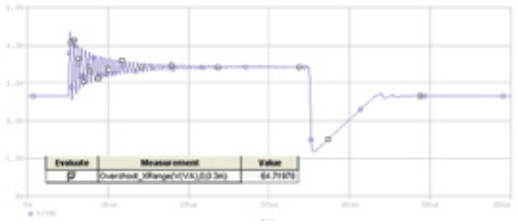


Figure 9 Transient Response

Conclusion

Is measuring the open loop Phase Margin enough to prove that a circuit is stable? In many cases the stability of a well-behaved linear circuit can be predicted using a small signal AC stability analysis, by measuring the circuit's open loop Phase Margin. The small signal analysis typically assumes that the circuit is linear around a fixed DC operating point. This assumption, in some cases, may not be accurate. Therefore, it would be wise and potentially more accurate to simulate the closed loop time domain response of the circuit, because in the time domain, the circuit's nonlinearities and DC operating points are simulated.

In this example a MOSFET presents a capacitive load that varies as a function of the DC operating point and is just one illustration showing why stability analysis in the time domain is prudent. One could imagine many similar situations involving other parts or conditions (like startup sequences, gain stage saturations, etc) in which a small signal AC analysis does not completely predict stability. Transient analyses can reveal valuable insight into a circuit's stability performance.

To download the PSpice files discussed in this article go to www.ema-eda.com/PhaseMargin.

Do you have an interesting topic you would like to share in EMA Currents? To learn more about this opportunity check out Page 10.

Moving from Altium to OrCAD

With Efren Taboada, an Electrical Engineer, located in Orem, Utah

EMA has encountered a number of customers moving from Altium products to Cadence OrCAD PCB design technologies throughout the year. To help the industry understand why this trend is occurring, we decided to talk with one of these customers to find out exactly what made them switch to the solutions provided by EMA.

One such customer is Efren Taboada, an Electrical Engineer located in Orem, Utah, who recently evaluated OrCAD and Altium this past June.

EMA: What were the main factors that led you to switch from Altium to OrCAD products?

Efren: The decision to switch to OrCAD was led by the productivity enhancements available with EMA's database management and PCB design solutions, the ability to cost-effectively accommodate my individual software needs, and the quality and dedication of EMA's support.

EMA: How does EMA's database management solution compare with Altium's?

Efren: EMA's database management solution was a huge differentiator for me as I was considering an alternative to Altium. The OrCAD Capture CIS/ Component Information Portal ™ (CIP) package allows me to search Digi-Key®, Newark®, and Future Electronics® part databases all at one time to check for part availability, before placing parts on my design. It also allows me to download parametric data from those distributor websites directly into my CIS database, without copying and pasting. There isn't any other solution that allows me to enhance my productivity like EMA's at this price point.

EMA: How does this make your job easier?

Efren: If I were using Altium's database management software, I would be forced to copy and paste all my parametric data manually. It would take an insurmountable amount of time to put all the footprints, schematic symbols, and parametric data in one place. To me, EMA's component management solution is priceless for my schematic capture process.

EMA: What are the advantages to the OrCAD PCB design solution?

Efren: OrCAD PCB design provides an added layer of error protection for PCB design work when compared with Altium's products. The OrCAD PCB design technology prompts you to think through your design as you are working. As a result, you are less prone to errors.

EMA: Was EMA able to provide a customized solution for your specific requirements?

Efren: EMA's products were flexible enough to accommodate my particular needs. Being able to scale the capabilities of the software to meet my particular needs was a huge advantge that can't be met by Altium without paying a high price.

"To me, EMA's component management solution is priceless for my schematic capture process."

EMA: Were you satisfied with EMA's technical support compared with Altium's?

Efren: I was very pleased. EMA's technical support was incredibly responsive and far more consistent with the quality of their support when compared with Altium. In just over a month, the support staff and I built a meaningful relationship with one another. I knew those assigned to me by name – Jeanine and Mac.

EMA: Do you think Altium serves a particular need in today's PCB design marketplace?

Efren: My opinion is, you might consider using Altium if you are willing to build your own libraries manually and have an ineffective way to interface with your supply chain and other departments within your company effectively. However, Altium simply doesn't have the professional capabilities offered to by EMA's solutions, especially when it comes to component management.

Do you find yourself in a similar situation with Altium technology? Don't hesitate to contact EMA for a personalized assessment of your unique challenges. Our services department is fully capable of assisting you with Altium to OrCAD design translations, database set-up, and training. Email Info@ema-eda.com.

Manny Marcano's Column in PCD&F

EMA's president and CEO, Manny Marcano, has recently been featured in Printed Circuit Design & Fab (PCD&F) magazine. His articles explore the topic of component data management(CDM) and Component Information Systems(CIS), a growing concern for many designers. Here's what Manny has covered so far:

May - Centralizing Component Libraries
This first installment introduces the topic of using a CIS by providing an informative anecdote about the inefficiency associated with working from individual libraries.

June - Corralling Chaos
In his second article, Manny presents his view on the best process to implement a CIS solution, and the dividends it pays over time.

August - Accurate BoMs, the First Time
This most recent article focuses on how an effective CIS improves the bill of materials, leading to a more accurate transfer of information among engineering, purchasing and manufacturing departments.

To read the complete articles click on their titles above.

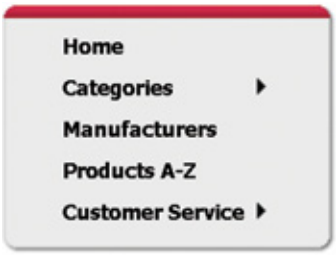
Also, read the article, Fundamentals of Component Data Management on Page 8

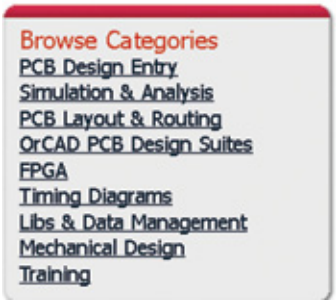
New: Shop Online at The EMA EDA Store

EMA recently launched an updated online store to provide you with even more access to product information. With products from Cadence®, Autodesk®, Aldec Inc®, AEi Systems®, DfM® and our own EMA EDA Solutions it has become increasingly important to organize it all. The new store presents these products so that decision makers can quickly and easily browse our solutions.

The new store allows you to search products in three different ways, either by category, manufacturer, or name (alphabetically). It also displays more concise product descriptions and makes comparing product options significantly easier.

Visit www.ema-eda.com/store/





Improving Design Time with CircuitSpace

With Troy Snow, Senior PCB Designer

CircuitSpace® offers advanced component placement and design reuse capabilities that expedite the PCB design process. Fully interoperable with Cadence OrCAD and Allegro® PCB design technology, it allows designers and engineers to significantly improve their cycle times and increase overall design quality, all with a solution that fits their budget.

PCB designers have relied on CircuitSpace to expedite their design process for several years. One such customer is Troy Snow, Senior PCB Designer with an Original Equipment Manufacturer (OEM) located in Austin, Texas, who has been using this software throughout his career.

EMA: What are the end products your company creates, and what software do you use for your PCB designs?

Troy: Our company designs high performance semiconductor test equipment for all kinds of memory products, such as USB drives, flash products, and other digital technologies. Our PCB designs range in size from a few square inches to over a square foot, and in complexity from 4 to as many as 18 layer stack-ups. Some of our smaller designs might have 100 or fewer parts, and some of the larger boards might have as many as 6,000 parts. We have used Cadence products exclusively for PCB design, including schematic capture, layout, and routing, for over ten years, and have recently upgraded to Cadence Allegro version 16.3. We had an outdated version of CircuitSpace at the time, and EMA helped us with an upgrade to that tool as well.

EMA: Can you describe your overall experience with CircuitSpace?

Troy: I have really enjoyed using CircuitSpace because of the increase in productivity it creates for myself and our design team as a whole. Different features help us eliminate manual, error-prone tasks, making the team more productive and significantly reducing the length of our design cycle. We use CircuitSpace on over half of our designs.

EMA: How does CircuitSpace augment your Allegro design flow?

Troy: Once I receive my net list from Allegro Design Entry HDL, I use CircuitSpace's AutoCluster™ feature to automatically group all my parts into functional, connected groups of components called clusters and place those groups on my board. Within minutes, all my chips, de-coupling capacitors, series terminations, and pull up/down resistors are linked together. I can then open a PDF of the schematic and see all my parts both grouped into their appropriate clusters and organized by schematic page. CircuitSpace will take all the components and then organize them by schematic sheet, which is a huge time-saver, especially when considering a design with four to five thousand parts and 80 to 100 or more schematic pages. These features save hours, if not days, in manual placement time for our team per design. With the click-of-a-button, I practically eliminate the process of manually placing and grouping parts together by schematic association.

"These features save hours, if not days, in manual placement time for our team per design."

EMA: What other features of CircuitSpace are useful to you and your design team?

Troy: The Replicate Cluster command has also been particularly useful to our team. Right now I have a 5,000 component design with several sections of the board that use similar circuitry. Once I have one circuit placed I am able to replicate the placement of the rest of these circuits automatically with CircuitSpace and then place those circuits like building blocks around a central FPGA. Analyzing the path of the rats nest, I am able to swap out the clusters until I get the arrangement that is the most efficient for routing. In some cases I can combine two clusters to build a larger circuit or merge clusters together before replicating. In many cases, I am able to combine groups of components into larger clusters with the push of a button and then replicate the placement and etch in similar clusters in a very short period of time.

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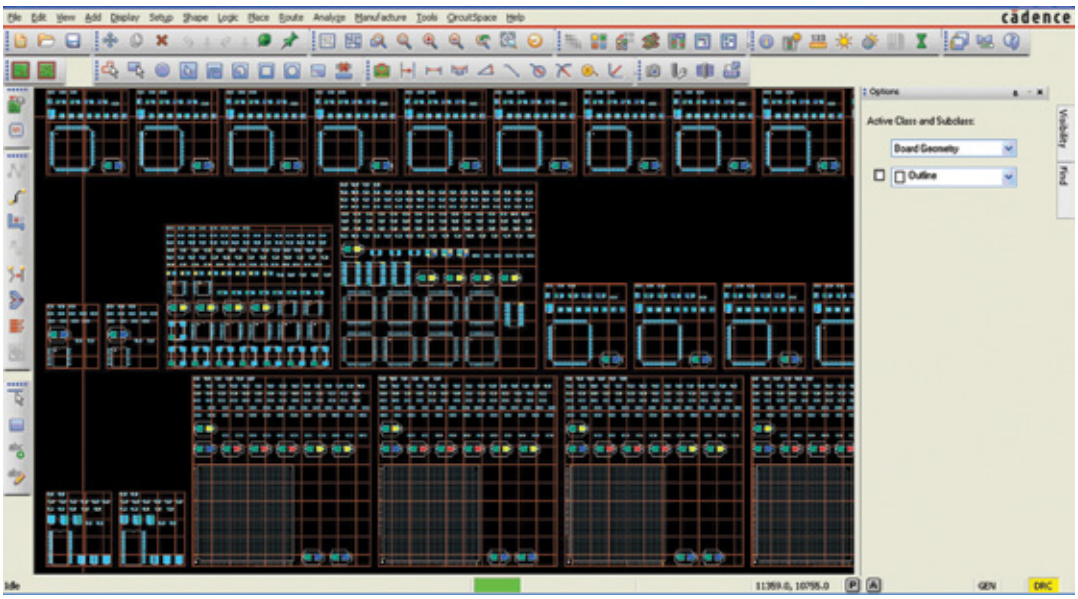


Auto-clustering with CircuitSpace groups components by logical properties for easier placement

EMA: How much time has this feature saved you?

Troy: There is no telling how much time I've saved with this feature. Being able to replicate clusters with two or three clicks, all in a matter of seconds, will probably save me days working on this particular design. Overall, the time savings offered by the various CircuitSpace capabilities are invaluable to our design time because much of the repetitive manual process can be eliminated. For example, I can swap the clusters of components around like building blocks, decide if I like the results or not, and then swap them back to their original positions if necessary. How do you quantify that capability? I don't know. All I can say is that CircuitSpace capabilities give the designer a lot of power to manipulate the placement of the components and the replication of etch with a speed and precision that would otherwise not be possible, saving countless hours in what would normally be duplicated manual effort for each individual circuit.

EMA: Are you satisfied with the support provided to you on this product from EMA?

Troy: For a small company like us, being able to tap into EMA's technical resources and personalized support is invaluable. EMA provides support for our entire design flow, all in one place. We were very impressed with the assistance they provided with our latest Allegro upgrade. Janine, an EMA Application Engineer, provided me with tutorials that were especially helpful during the migration process to version 16.3. It is refreshing to be a phone call away from immediate assistance, as opposed to filtering through online forums or working with support centers halfway across the world.

EMA: Would you recommend CircuitSpace to other PCB designers?

Troy: ABSOLUTELY. In fact, several years ago I recommended CircuitSpace while employed with a different company. The lack of access to CircuitSpace's automated component placement and circuit replication capabilities had a very negative impact on my productivity. CircuitSpace is well worth the additional investment for any engineering team with moderate to complex designs.

For more information on the latest features and pricing for CircuitSpace, please visit www.ema-eda.com/circuitspace. An on-demand demo is available on this webpage that will demonstrate CircuitSpace's capabilities. You can also watch a video demonstrating the automated component feature in CircuitSpace.

Stay Connected with EMA

EMA's LinkedIn page is a great way to stay up-to-date on the latest news and discounts from EMA, network with people in similar industries and provide valuable product reviews to benefit everyone.

For Twitter users, one page has been created for those involved with EDA (www.twitter.com/ema_eda) and another has been created for those involved with MCAD (www.twitter.com/ema_mcad). These two pages provide information on all the EDA and MCAD technologies sold and supported by EMA.

For YouTube users EMA's Channel (www.youtube.com/EMADesignAutomation) contains videos focused on all the technology sold and supported by EMA, as well as product integrations and enhanced capabilities provided to users of OrCAD technology.

Follow EMA on any of these sites to stay connected with us.

Component Information Portal (CIP) Version 4.2

EMA's Component Information Portal offers an advanced component data management solution to our users. If you are unfamiliar with CDM an explanation can be found in the article, "Fundamentals of Component Data Management", conveniently located on this page. The message is clear, CDM keeps you organized.

CIP Version 4.2 Highlights

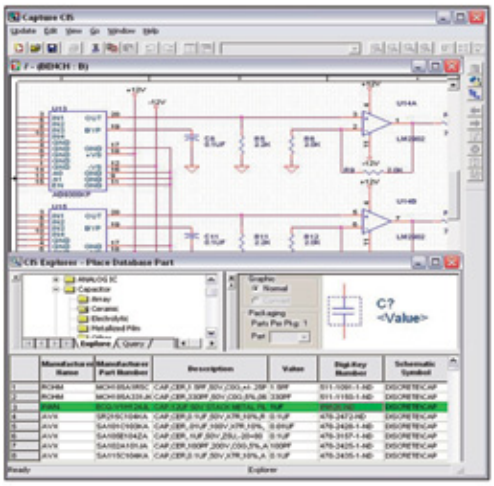
Arrow Electronics® integration:
CIP users have access to all the latest up to date part information from one of the world's leading technology suppliers

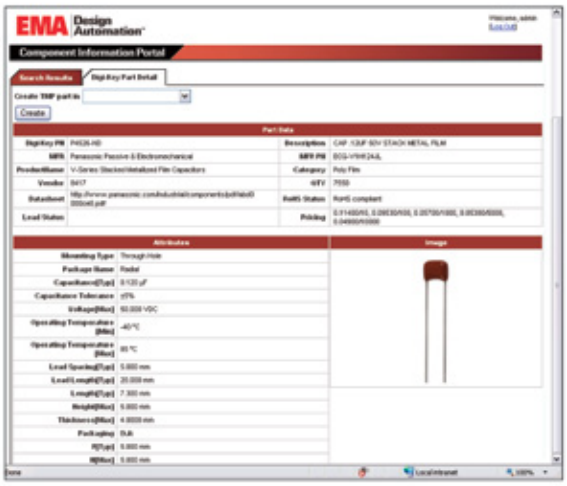
Order of Part Number:
Pull-down list can be configured by an administrator for ascending or descending order

CSV file formats:
Can be configured to use semicolon as the delimiter to support international formats

Distributor sync:
Allows distributors to be synchronized individually

For more information on CIP, www.ema-eda.com/CIP4.2 call 877-362-3321, or email info@ema-eda.com.





Fundamentals of Component Data Management

Adapted from Clive "Max" Maxfield

If you are not exactly sure what Component Data Management (CDM) really is, or why it is important to you as en electrical engineer, you are reading the right article at the right time in your career.

This article focuses on CDM in the context of designing and building printed circuit boards. Whether a circuit board is large or small, it is going to incorporate a variety of components. A simplified view of CDM is a process of managing the components used on a PCB, all the way through the board's development process. This starts with the original component selections made by the design engineers, and continues through the board layout to verification, component procurement, design-for-manufacture, and finally board population and assembly.

Types of CDM

CDM can take many forms based on the level of sophistication. The lowest form could be a pencil and paper listing of component details; it's hard to imagine much scalability with this method. An improvement could be an electronic spreadsheet document; accuracy issues arise with sharing and updating of the document. The best possible solution is a CDM information system that stores all component-related information and is accessible and updatable by everyone in the development team.

Benefits of CDM

CDM reduces the risks of error associated with the project by ensuring everyone is working with the same data. This increases efficiency because of the time saved checking for errors or fixing them. Also, it eliminates repeated data entry because components are stored in a library.

In the cases where multiple designs are using similar components, the component data management system can help to ensure all boards use the same component. This allows procurement to seek greater economies of scale and increase margin.

Accurate information on prices and availability help to ensure that the board can be manufactured and assembled as planned. This reduces the chance of having to unexpectedly swap out a component or re-spin the entire board, both of which impact costs and introduce delays. This results in reduced time to market and, more importantly, reduced time to profit.

To read this article in it entirety visit www.ema-eda.com/documents/Component_Data_Management.pdf

For more info on EMA's CDM Solutions visit www.ema-eda.com/CDM

Select The EMA Start Page in OrCAD Capture

Overview of Start Pages

Cadence has added a new start page to OrCAD Capture that allows you stay informed about latest releases and recieve personalized information from your prefered channel partner about events, training, industry news, and much more. By selecting EMA you will give yourself a convienient way to stay connected to the PCB world. This start page is another way to take advantage of EMA's outstanding post-purchase support.

Contents of the EMA Page

- Find out about new apps
- Discover design solutions
- Get training information
- Learn about upcoming events
- Contact support
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Getting Started

Try it out for yourself by selecting EMA from the partner dropdown list in the center of the customize page or in the lower right corner of the current start page.

For more information contact info@ema-eda.com.

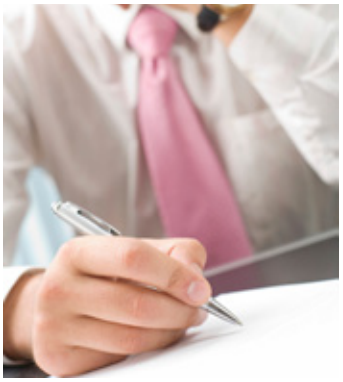
Webinar: PSpice Advanced Options

Join EMA for the next installment of our PSpice webinar series. This session will take you beyond the basic features of Cadence® PSpice® technology discussed in our Tips 'n Tricks webinar. During this webinar, EMA will show you how advanced features in Cadence PSpice A/D and Cadence PSpice Advanced Analysis will save you time and increase productivity during the simulation process.

Webinar attendees will learn:

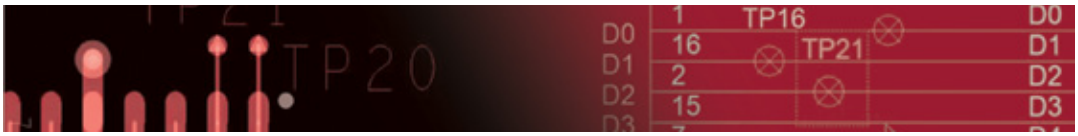
- How to utilize the advanced features in PSpice A/D and PSpice Advanced Analysis to increase reliability of circuits.
- How to simulate more in less time with automated analysis
- How to perform behavioral modeling with Analog Behavioral Models (ABM)
- How to optimize circuit for performance while also designing for cost

We hope you will take this opportunity to enhance you knowledge of the new software. To begin go to the URL below www.ema-eda.com/webinar



Content Wanted

Have you ever wanted to share some of your experience with the engineering community? Have a topic you would really like to spout-off about? How would you like to get paid to do just that? Here is your chance to get your name in front of thousands of engineers. EMA is looking for technical writers to contribute articles for publication. We are looking for articles, technical tips, short tutorials, and white papers on current technologies and techniques centered on the Allegro platform and OrCAD PCB design technologies. If this sounds like something you would be interested in, please contact us at info@ema-eda.com for all the details.



Taking Advantage of TCL/TK Scripting Capability

With Bruce Smith from Aclara RF Systems

As part of the Cadence OrCAD 16.3 release, Cadence OrCAD Capture was enhanced to include support for TCL/TK scripting capability. With this new capability, designers can apply automation to manual processes and complete projects more quickly. It also allows users to create custom features that do not exist natively, further enhancing and extending the OrCAD Capture environment.

Bruce Smith from Aclara RF Systems, Inc. in Solon, Ohio is one customer that has taken advantage of this new functionality. Aclara creates products that assist with device networking, data-value management, and customer communications to water, gas, and electric utilities.

EMA: Describe the problem you were facing that was ultimately solved by the new TCL/TK scripting capability in OrCAD Capture.

Bruce: I was looking for a way to back-annotate test points placed in the PCB Editor to a Capture schematic sheet. Defining test points at the schematic level helps facilitate logic troubleshooting during the manufacturing process. The issue of placing test points in the schematic is that they then become individual single pin components that you have to place manually in the PCB design, and then route (there could be hundreds of these in a design). The manual labor required for this task is very time consuming and error-prone, and I thought we could automate the process using a script.

"I was looking for a way to back-annotate test points placed in the PCB Editor to a Capture schematic sheet."

EMA: Why are test points important in a design?

Bruce: Almost all PCBs go through some type of testing after manufacture and/or assembly. Test points are contact land patterns or holes (usually vias) on one or both sides of the PCB that are designed to allow convenient access to what would normally be inaccessible locations, particularly after assembly. They are used to find open or short circuits at the bare-board stage, perform in-circuit tests, functional tests or troubleshoot a returned assembly for repair.

EMA: How was our services team able to assist you with this?

Bruce: Due to my workload here at Aclara, I simply did not have enough time to become familiar with TCL to work on this. I asked the services team at EMA to develop a TCL script to automate this back-annotation process. The script extracts the netname and test point reference designator from OrCAD PCB Editor and places it into a separate notepad file. When the user clicks on a net in OrCAD Capture, the script extracts the net name and coordinates of the mouse pick point from the file. Based on this information, it then places a test point symbol on the net with the correct reference designator.

EMA: Did our service team's solution meet your expectations?

Bruce: They did meet expectations, and also, added additional functionality to the system.

EMA: Describe your new test point creation flow?

Bruce: Our new flow involves creating test points automatically at the PCB design stage using the automated test prep utility in Cadence Allegro (and now in OrCAD PCB Professional as of release 16.5!) and then back annotating this data to the schematic with the app created by EMA. This saves us from individually creating and manually placing each of what could be hundreds of test points while still giving us the ability to see the test points in the OrCAD schematic.

EMA: How does our test point features compare with other software?

Bruce: I think most competitors have auto test point generation at the PCB design level, but I don't know of any that back annotate these test points to the schematic like EMA does.

Continued on page 11>

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Did you know?

There are added functions in the Cadence Test Prep utility such as selecting the pin or pad type, numbering and displaying the TP text, defining the layer, test method or bare board methodology, test grid, minimum pad size, TP via substitution, allowing test directly on a trace, allowing pin escape, and fixing or unfixing test points for fixture preservation during an ECO, that make the Cadence Test Prep feature stand alone.

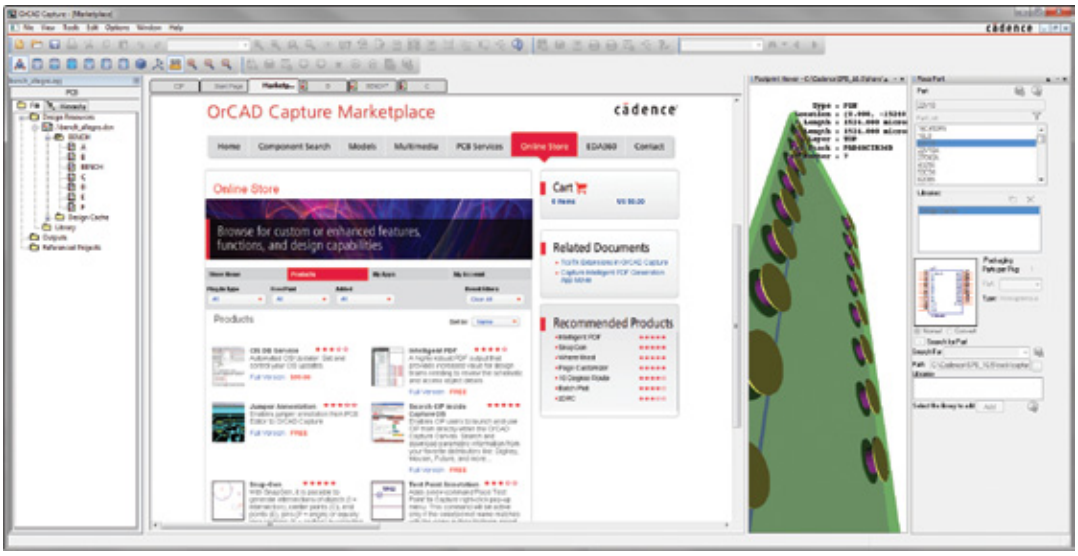
The automated test point annotation capability described in this customer success story is now available as the TestPoint Annotation App in the new OrCAD Capture Marketplace. To learn more about the marketplace, and some of the initial apps available, check out the article below.

For more information on the TCL/TK scripting capability and how EMA can customize your OrCAD software to your specific needs call 877-362-3321, or email info@ema-eda.com

Cadence Unveils OrCAD Capture Marketplace

The OrCAD Capture Marketplace is a unique Web-enabled environment that brings a complete PCB ecosystem—including an industry-first online store for applications—to engineers' fingertips. Accessible within the new version of the Cadence OrCAD Capture schematic design tool, the marketplace fundamentally changes the way PCB designers can access design data. It allows them to stay informed and discover new resources, including apps to customize and extend the OrCAD environment.

The Marketplace has On-demand access to information, design data, and resources from across the Web at the click of a button. Users get a design environment from which they can efficiently conduct research to locate essential materials, and easily access the latest design or OrCAD-centric know-how.



The OrCAD Capture Marketplace offers two key advantages for PCB designers. The first advantage is productivity through convenience.

The second advantage is an extensible and customizable design environment. Within OrCAD Capture Marketplace, users will have access to an online store where they can find and download apps, from Cadence and EMA Design Automation.

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CircuitFit App for OrCAD Capture

EMA is participating in the launch of the OrCAD Capture Marketplace with a number of initial apps geared towards personal productivity. One app we are particularly proud of is CircuitFit.

CircuitFit helps engineers early in the design process by giving them estimates of how much space they will need based on desired functionality. This helps answer important questions:

Will my design fit on the board space available?

How much routing room will I have?

Do I need to change the board size to maintain functionality?

Do I need multiple boards?

Should I be looking at smaller form factor parts?

Can I use multiple inexpensive devices in place of one compact, expensive component?

For more information on apps Visit www.ema-eda.com/Apps

Watch a Video on CircuitFit

App Development Services

Looking for customization of your OrCAD environment? Have an idea of something you wish you could do? The EMA apps development team can help. Contact info@ema-eda.com for more information.

OrCAD PCB Classroom Training

Increase your PCB design productivity by attending our in-depth, hands-on classroom training sessions. All our classroom courses are taught by professional instructors with years of training and application experience. Learn more at www.ema-eda.com/classroom.

EMA classroom training is coming soon to these cities:

Baltimore, MD

Westford, MA

Huntsville, AL

We also offer Virtual Classroom Training, for details visit www.ema-eda.com/training/

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Web: www.ema-eda.com

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These applications will enable enhanced control of the users design processes and flows through new features or capabilities. By providing all the necessary resources to take a design from concept to final board implementation, OrCAD Capture Marketplace provides access to a rich design ecosystem in a new delivery model.

Watch the Cadence OrCAD Capture Marketplace Overview with Josh Moore, Director of Product Marketing for OrCAD.

For more information on the OrCAD Capture Marketplace, please visit www.ema-eda.com/Apps Call 877-362-3321, or email info@ema-eda.com.

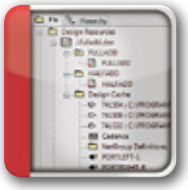
Convienient, Powerful, Options

CIP in CIS
Instant access to search and download component data for millions of parts.

ShapeUtils
Simplify the process of creating and editing shapes in the PCB Editor.

OrCAD PDF Generators
Share your designs with non-CAD users through intelligent PDF generators.

TestPoint Annotator
Sync test point placement between OrCAD PCB and Schematic.



Find in Design
Quickly search for common values across multiple schematics and projects.

Status Display
Avoid errors with fully customizable visual indicators of properties.

LabelTune
Automatically adjust PCB Editor RefDes labels to match part orientation and size.

SymbolGen
Build and verify OrCAD schematic symbols in a fraction of the time.

CircuitFit
Perform early fit studies at the schematic level before you commit to placement.