Stability Analysis of Multi-Output Switching Power Supplies Using State Average Models in Analog Workbench

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Abstract

Loop stability analysis using state average models has been well documented. State average models have been developed in Analog Workbench, which facilitate the stability analysis of switching power supplies. This paper will attempt to address the development, use and limitations of these state average models in comparison with the measured open loop response of a multi-output switching power supply.

I. Introduction

Models for switching power supples are getting significantly more sophisticated as topologies change. The trend seems to indicate that computer models must become more accurate and faster to run. Analog Workbench seems to have found a niche in the power supply modelling area via the use of its state average models. It has been especially useful in the area of stability analysis because of its ability to perform worst case analysis as a function of phase and gain margin on single our multiple output power supplies. However, new and more accurate models are still needed so that power supply stability can be better understood and evaluated.

II. What is ...

To better understand the use of the analysis tools we must first understand the language of power supply stability. Therefore, a series of "what is" questions and answers are present below to assistance us in understanding stability as it relates to power supplies.

What is stability? This question may seem somewhat trivial in nature but many designs start off being unstable. Therefore, a closer look may be in order. Stability is defined as the operational condition of a circuit which results in no unwanted oscillations when excited by any stimulus or gain variations. In reality we consider circuits "unstable" even if the oscillations get dampened out. A circuit is said to be stable if it has adequate gain and phase margins.

What is gain and phase margin? Phase margin is defined as the difference between 180° and the phase at the crossover frequency for the open loop frequency response. A positive phase margin of 45° is typically considered acceptable. Gain margin is defined as the absolute value of the number of dB below 0dB when the phase is equal to -180° for the open loop frequency response. Typically a 6dB gain margin is reasonable. Both gain and phase margin can be measured with a marker in the Network Analyzer in Analog Workbench.

What is a the crossover frequency? The crossover frequency is the frequency at which there is unity gain or 0dB.

What is the open loop frequency response? The open loop frequency response is made up of two parts; a phase and gain response. Phase is expressed in degrees and gain is expressed in dB. The frequency response is often referred to as a Bode plot. The Bode plot is displayed on the Network Analyzer with one channel displaying magnitude in dB and one channel displaying phase in degrees.

What is the closed loop frequency response used for? A closed loop response can also be used to determine the stability of a power supply but instead of plotting phase and magnitude the closed loop response is plotted on a plane which displays the real and imaginary values. This plot is called a Nyquist or Root Loci plot.

What is a state average model? As has been defined in many references a state average model is a model which replaces the cycle by cycle switching of a power supply with an average model of what that cycle by cycle switching would normally produce. For example, if a switching module had a 50% duty cycle to achieve the desired output voltage the state average model would replace the 50% duty cycle with a DC gain of 0.5.

III. How is or does ...

Now that the "what is" questions are answered it is necessary to understand the "how" of stability analysis. Again the questions and answers that follow should help us better understand stability by showing how it is evaluated and what causes it.

How is the open loop response determined? An open loop response requires that the loop be broken or opened somewhere. The typical place to "break" the loop on a power supply is at the error amplifier.

How is an unstable design stabilized? In stability is caused by a lack of phase or gain margins. To increase these margin compensation can be added to provide in the form of RC network around the crossover frequency.

How does output and input impedance effect stability? There is a relationship between the output impedance of the power supply and the output impedance of the input filter. The input filter's input impedance is generally designed to filter the power line. Its output impedance may in reality be rather poor with no significant dampening. The output impedance of a switching power supply is negative. Therefore a stability problem may exist if the input filter's output impedance is less than the absolute value of the output impedance of the power supply.

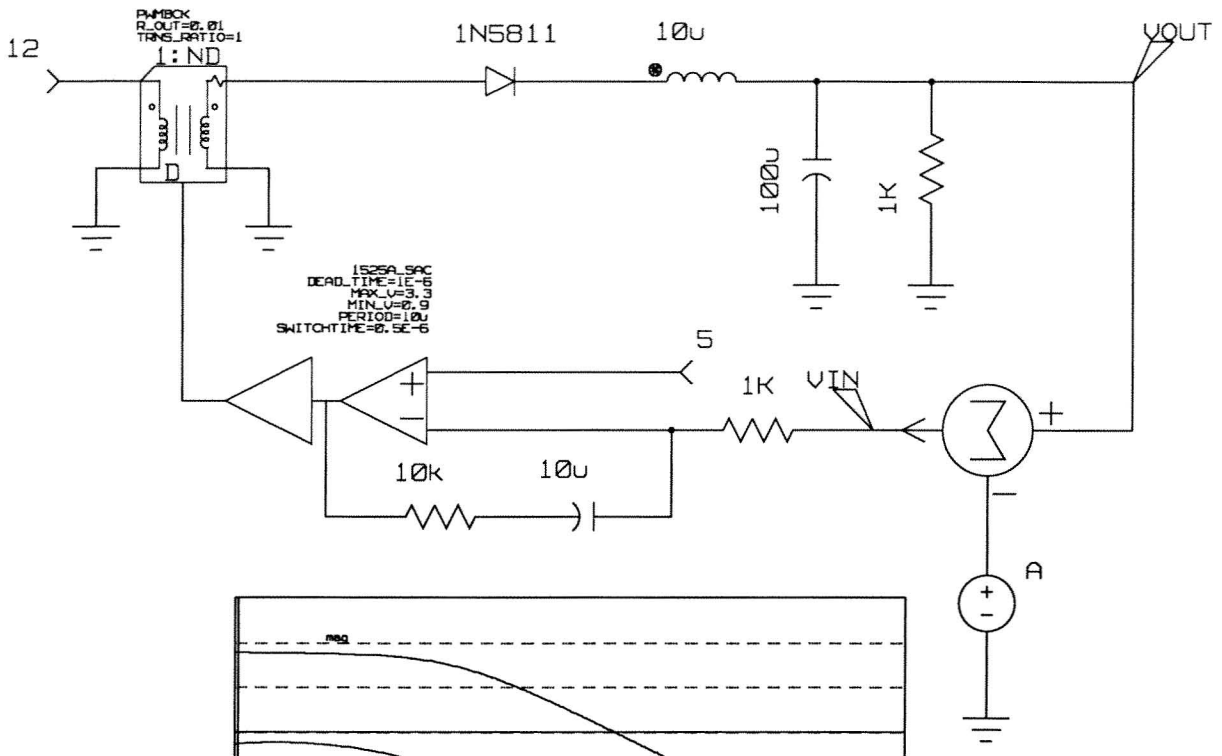
How does a capacitor's esr change the open loop response? The output capacitor's esr (equivalent series resistance) will typically introduce a high frequency pole which is usually above the crossover frequency. It effects could include reducing gain margin. (See Figure One.)

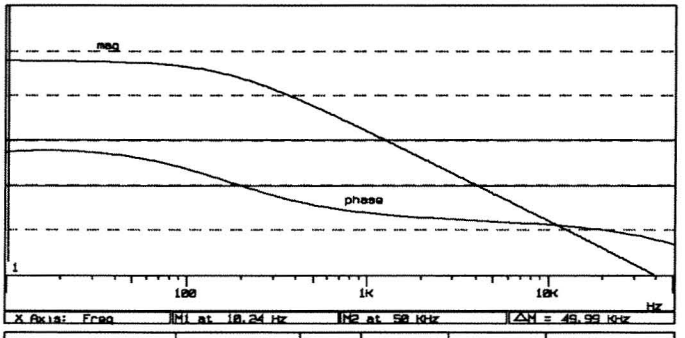
How does an inductor's esr change the open loop response? The ers of the output inductor will typically have little affect on the small signal analysis, stability. However it can change the bandwidth slightly. (See Figure One.)

How does a diode's forward voltage drop change the open loop response? Like the esr of the output inductor it has little impact on loop stability but it can greatly effect the efficiency and regulation of the power supply.

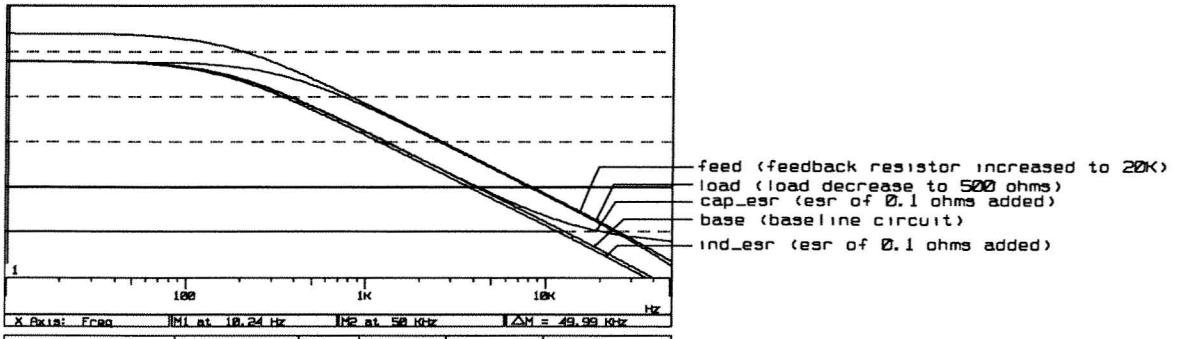
How does a modulator's open loop response change the open loop response of the overall power supply? The modulator generally has more gain than is needed. It's affects on loop stability are very significant because the majority of the DC gain can be found in this stage. Also, stabilization of a loop is usually accomplished by compensation of the modulator's error amplifier. (See Figure One.)

How does an a change in load change the open loop response? The load can radically change the stability of the power supply by moving the crossover frequency and thus change the gain and phase margins. Also, load extremes could decrease the inductor current to be discontinuous and dramatically change the open loop response. (See Figures One and Two.)





Channel		Display	Cmplx	Scale/div	Func	Value
1 Net Set	ON	PRB(VOUT)/PRB(	MAG	10.000 d	phasemarg	89.929 deg
2 Net Set	ON	-PRB(VOUT)/PRB	PHASE	50.0 deg	M1	-13.0 deg
3 Net Set	OFF	C1	MAG	10.000 d	zero_cross	4.0021 KHz
4 Net Set	OFF				gainmarg	48.675 dB



Channel		Display	Cmplx	Scale/div	Func	Value
9 Net Set	ON	base	MAG	10.000 d	M1	28.003 dB
10 Net Set	ON	cap_esr	MAG	10.000 d	M1	28.002 dB
11 Net Set	ON	feed	MAG	10.000 d	M1	34.230 dB
12 Net Set	ON	load	MAG	10.000 d	M1	28.015 dB
13 Net Set	ON	ind_esr	MAG	10.000 d	M1	27.990 dB

Figure One
State Average Model

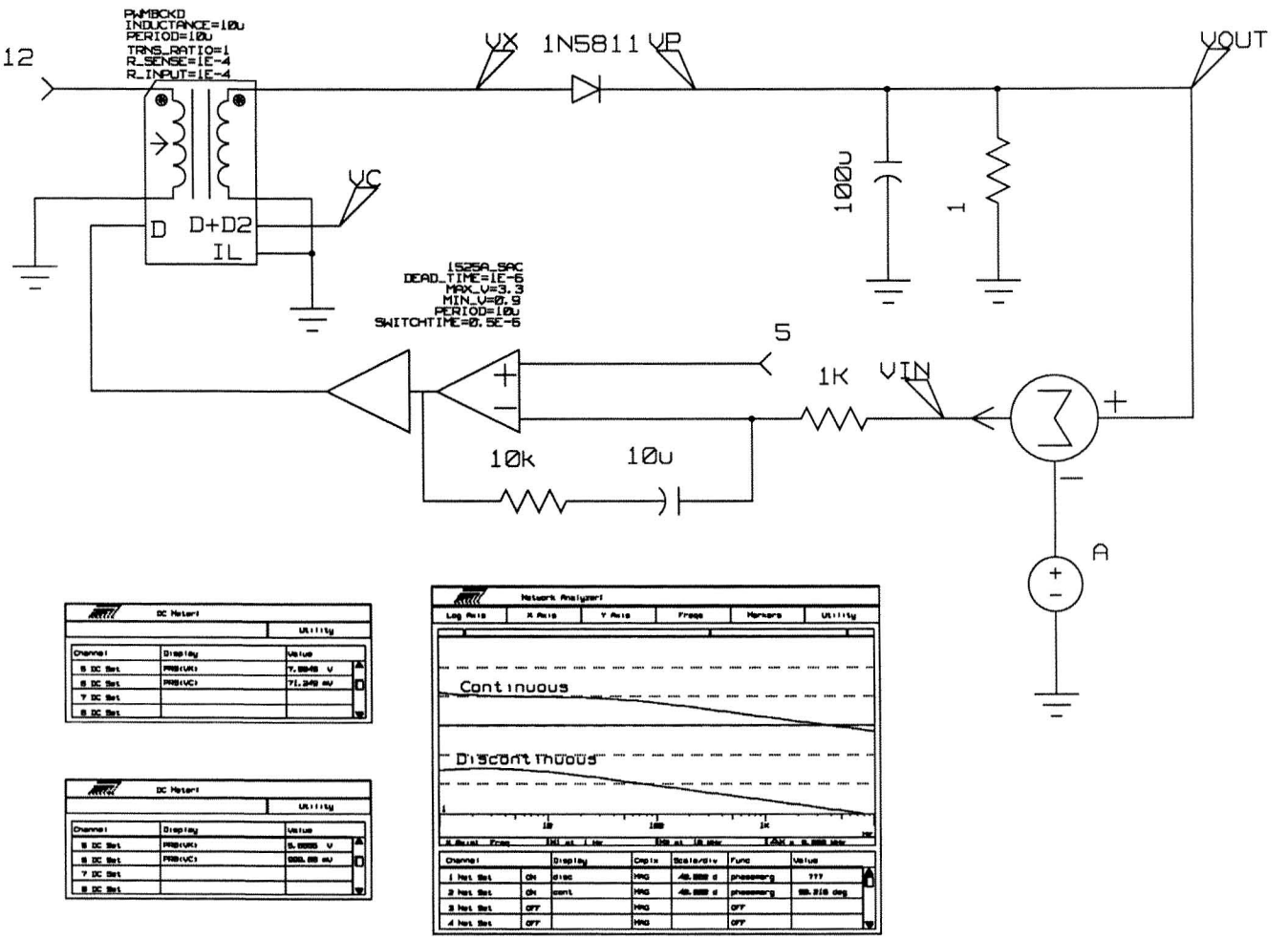


Figure Two
Discontinuous Inductor Current

IV. The Example

Recently it was necessary to model four multi-output switching power supplies on Analog Workbench so that a worst case stability analysis could be performed. The power supplies are scheduled to be used on a weather satellite and their stability is essential for the overall success of the weather instruments.

The following steps were used to develop the stability models:

Step One - The first step taken to model the power supplies was to develop a set of component models. The component models detailed how the components would change over temperature, aging, radiation as well as their initial tolerance. (Page 2 of Figure Three shows the component values.)

Step Two - Next, parameters which would be pertinent to a stability analysis, i.e. dead time, efficiency, etc. were determined. These parameters were in some cases the results of other worst case analyzes. (Again, page 2 of Figure 3.)

Step Three - Test data was collected on the power supplies to assist in the power supply model correlation. The open loop frequency response, output regulation, efficiency and other pertinent information was collected. (Page 3 of Figure 3 shows some of the data that was used to correlate the model to.)

Step Four - A state average model was developed based on the first three steps. The output transformer was modeled with multiple DC to DC transformers who's primaries were paralleled. The output inductors were reflected to the primary of the power transformer and entered into the PWMBCKD and 1846_SAC models as "inductance". The loop was broken in the same place as was done during test. The other dc loses were lumped together and added to the power supply model. (Page 1 of Figure 3 is the state average model of the multi-output power supply.)

Step Five - The models were correlated by comparisons between both the DC and open loop AC responses. Once this step was completed the model was considered acceptable for the worst case analysis and Sensitivity, Parametric Plots and Monte Carlo Analysis was performed on the power supply model. (Results are shown on page 3 of Figure 3.)

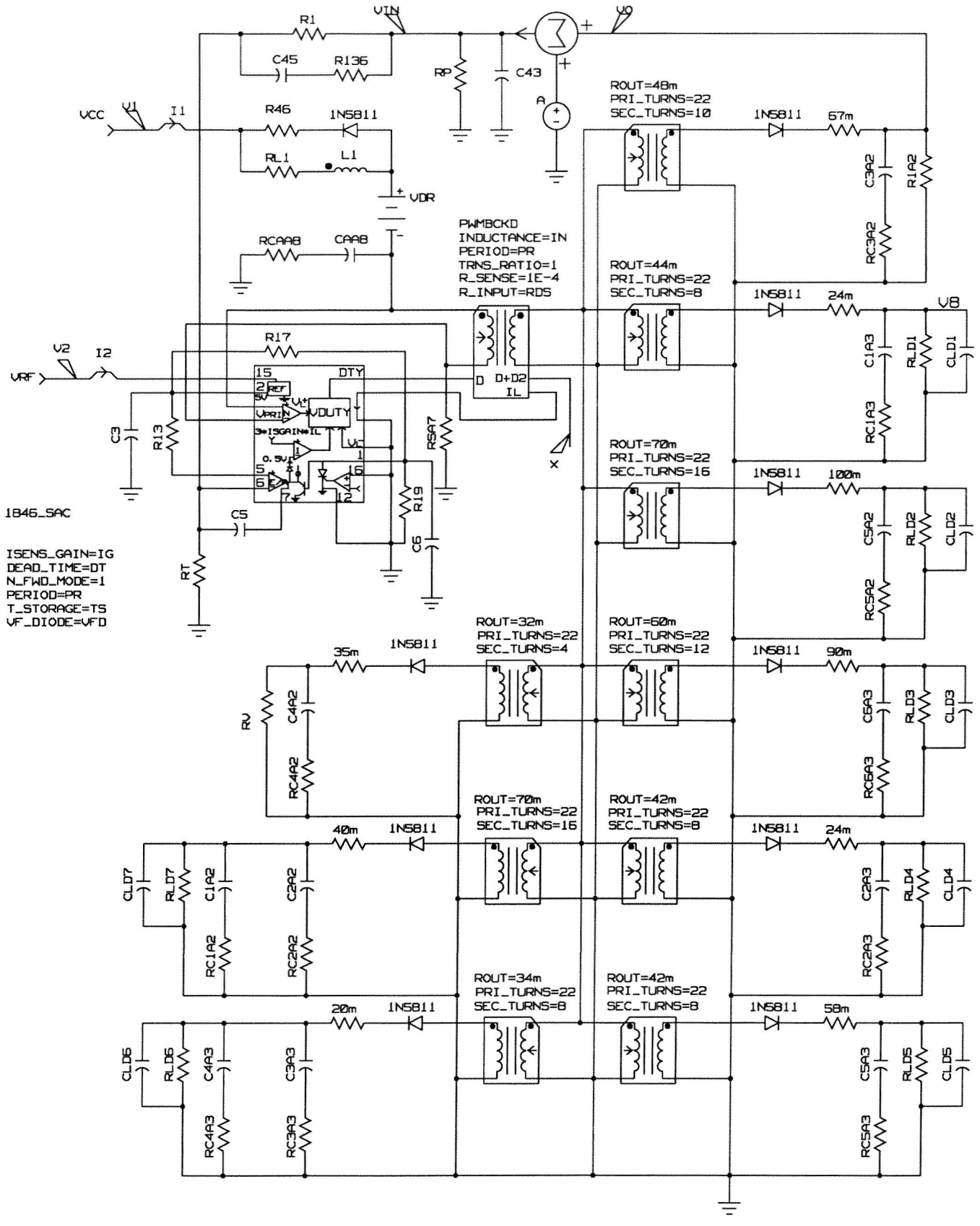


Figure Three
Multi-Output
State Average Model

TITLE: MULTI-OUTPUT PS WCA - STABILITY STATE AVERAGE MODEL	DATE: 6 JULY 1993
ENGINEER: A. G. BELL	PAGE: 1 OF 3

Default Variables:

Tempcos (ppm):
RTMPA=0
RTMPQ=0

Tolerances:
RTOL=0
CTOL=0
LTOL=0
VTOL=0
ITOL=0

PRTHS=IP
PARVAR=TRUE

Smoke Limits:
RMAX=.25
CRMAX=0.005
RTMAX=200

CMAX=50
CRMAX=125
CSMAX=0.005
CTMAX=125
CIMAX=1
LMAX=5
VMAX=300
IMAX=1
VMAX=100

⊕ User Variables:

CS=7.552e5, 70.3%, 41.4%, FLAT
IN=147e-6, 15%, 15%, FLAT
C6A3=10E-6, 39.7%, 39.7%, FLAT
RC6A3=1.20, 60%, 60%, FLAT
C5A2=47E-6, 39.7%, 39.7%, FLAT
RC5A2=0.7, 60%, 60%, FLAT
C2A2=47E-6, 39.7%, 39.7%, FLAT
RC2A2=0.7, 60%, 60%, FLAT
C1A2=47E-6, 39.7%, 39.7%, FLAT
RC1A2=0.7, 60%, 60%, FLAT
C4A2=47e-6, 39.7%, 39.7%, FLAT
RC4A2=0.7, 60%, 60%, FLAT
C2A3=350E-6, 39.7%, 39.7%, FLAT
RC2A3=0.24, 60%, 60%, FLAT
C1A3=350E-6, 39.7%, 39.7%, FLAT
RC1A3=0.24, 60%, 60%, FLAT
CAA8=344E-6, 39.7%, 39.7%, FLAT
RCAA8=0.08, 60%, 60%, FLAT
C6=10E-6, 15.24%, 15.24%, FLAT
C3A2=0.27E-6, 15.24%, 15.24%, FLAT
RC3A2=2.19, 60%, 60%, FLAT
L1=3.07e-6, 12%, 12%, FLAT
RL1=5E-3, 15E-3, 3E-3, FLAT
VFD=0.81, 22.62%, 22.62%, FLAT
TDT=720E-9, 23%, 23%, FLAT
DT=0.9*TDT
TS=0.1*TDT
RLD1=24.3, 98.3, 13.929, FLAT
RLD2=58.9, 220.3, 31.171, FLAT
RLD3=96.2, 180.3, 72.123, FLAT
RLD4=26.8, 37.4, 19.979, FLAT
RLD5=23.2, 99.3, 9.634, FLAT
RLD6=27.2, 23.8, 21.336, FLAT
RLD7=58.5, 99.2, 40.245, FLAT
CLD1=636e-6
CLD2=184e-6
CLD3=160e-6
CLD4=625e-6
CLD5=64e-6
CLD6=1200e-6
CLD7=65e-6
RDS=0.141, 32.6%, 32.6%, FLAT
C5=1020E-12, 43.54%, 43.54%, FLAT
C3=0.047E-6, 43.54%, 43.54%, FLAT
C43=0.1E-6, 43.54%, 43.54%, FLAT
C5A3=100E-6, 39.7%, 39.7%, FLAT
RC5A3=0.53, 60%, 60%, FLAT
C3A3=100E-6, 39.7%, 39.7%, FLAT
RC3A3=0.53, 60%, 60%, FLAT
C4A3=100E-6, 39.7%, 39.7%, FLAT
RC4A3=0.53, 60%, 60%, FLAT
R19=2.43E3, 3.1%, 3.1%, FLAT
R13=51.1E3, 3.1%, 3.1%, FLAT
R46=100, 3.1%, 3.1%, FLAT
R1=100E3, 0.0522%, 0.0522%, FLAT
RT=68.5E3, 0.0522%, 0.0522%, FLAT
R136=2.61E3, 2.02%, 2.02%, FLAT
R17=1.5E3, 2.02%, 2.02%, FLAT
C45=5600E-12, 1.18%, 1.18%, FLAT
RP=500, 2.38%, 2.38%, FLAT
IG=0.1, 2.38%, 2.38%, FLAT
RSA7=IG
R1A2=1E3, 2.38%, 2.38%, FLAT
VDR=0.486, 29.15%, 29.15%, FLAT
VCC=40, 3.0, 2.0, FLAT
VRF=VCC/3.3333
PR=4.587E-6, 0.01%, 0.01%, FLAT
RV=3.1

Figure Three
Multi-Output
State Average Model

TITLE:MULTI-OUTPUT PS WCA - STABILITY STATE AVERAGE MODEL	DATE: 6 JULY 1993
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DC Meter: MULTI_PS

Utility

Channel	Display	Value
1 DC Set	SIG(V8)	9.7469 V
2 DC Set	PRB(V1)*PRB(I1)	41.426 W
3 DC Set	C5+C6+C7+C8+C9+C10+C1	31.309 W
4 DC Set	C3/C2	755.79 m

DC Meter: Measured Data

Utility

Channel	Display	Value
Value 1	V8 Voltage	9.57
Value 2	Efficiency (MIN)	75%

DC Meter: MULTI_PS

Utility

Channel	Display	Value
5 DC Set	PWR((MLT RSS109P))	3.9095 W
6 DC Set	PWR((MLT RSS110P))	6.9271 W
7 DC Set	PWR((MLT RSS102P))	2.3501 W
8 DC Set	PWR((MLT RSS84P))	3.5508 W

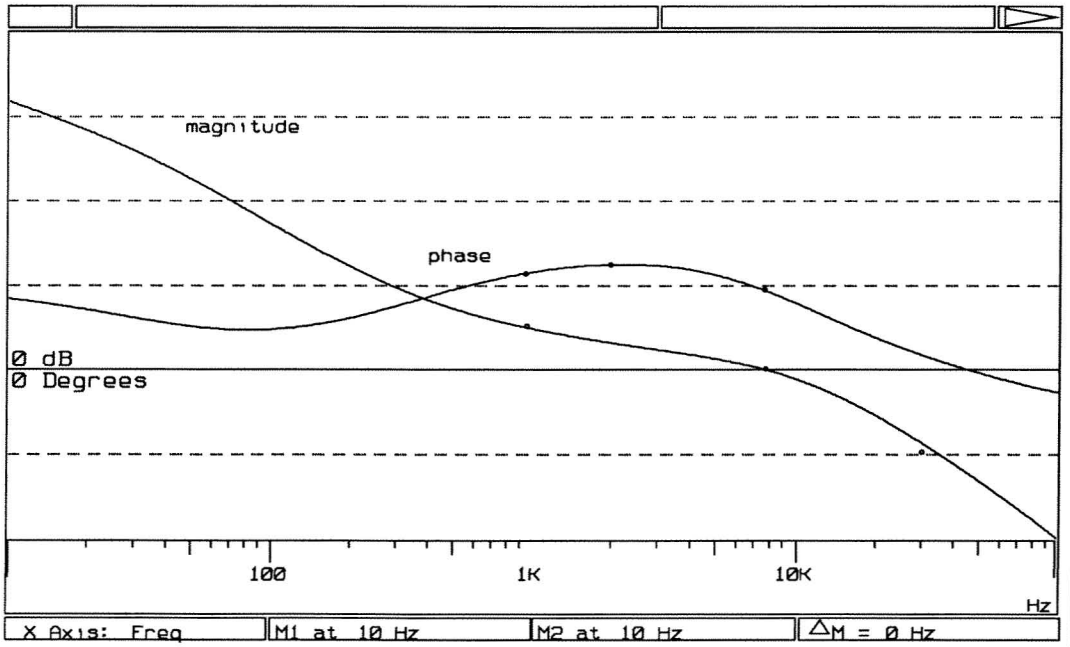
DC Meter: MULTI_PS

Utility

Channel	Display	Value
9 DC Set	PWR((MLT RSS85P))	4.0007 W
10 DC Set	PWR((MLT RSS2P))	3.5025 W
11 DC Set	PWR((MLT RSS4P))	6.9882 W
12 DC Set		

Network Analyzer: MULTI_PS

Log Axis | X Axis | Y Axis | Freqs | Markers | Utility



X Axis: Freq | M1 at 10 Hz | M2 at 10 Hz | ΔM = 0 Hz

Channel		Display	Cmplx	Scale/div	Func	Value
1 Net Set	ON	PRB(VO)/PRB(V	MAG	20.000 dB	phasemarg	95.983 deg
2 Net Set	ON	PRB(VO)/PRB(V	PHASE	90.0 deg	OFF	
3 Net Set	OFF	C1	MAG	20.000 dB	zero_cross	7.7623 KHz
4 Net Set	OFF				gainmarg	25 dB

Figure Three
Multi-Output
State Average Model

TITLE:MULTI-OUTPUT PS WCA - STABILITY STATE AVERAGE MODEL	DATE: 6 JULY 1993
ENGINEER: A. G. BELL	PAGE: 3 OF 3

As can be seen on page 3 of Figure 3 the state average model closely correlates to the measured open loop response. Therefore, the model is validated and can be used in the worst case analysis.

V. Conclusion

This paper has attempted to explain some of the factors which are associated with stability as it relates to switching power supplies. Numerous questions and answers were discused and an example model of which was correlated to test data of a multi-output power supply was given. In addition, the steps that could be followed to develop a state average model which can be used to investigate power supply stability was enumerated. Power supply stability will continue to be a challenge to design and analyze but as more models and tools are developed other concerns in addition to stability can be investigated.

VI. Other Items

Other topics germane to power supply stability such as subharmonic oscillations, current loop stability, high frequency accuracy, noise, input impedance and saturation of gain stages would require addition study to determine their significance on stability. New models which address some of these topics are being developed and should be integrated into our power supply models and understand as they mature.

VII. Dedication

I would like to dedicate this paper to my new baby daughter Elisabeth Ann Bell. She was born during the preparation for this paper and has inspired to do my best.

VIII. References

1.) Switching Power Supply Control Loop Design by Lloyd Dixon, Oct 91.

2.) New Modeling Tools Improve PWM Analysis and Design: Part I & II by Raymond Ridley, PCIM Jan & Feb 1990

3.) The Essentials of Stable Power Supply Design by Raymond Ridley, High Frequency Power Conversion Conference 1993, Session 8

4.) Designing Multi-Output Power Converters by Charles Mullett, Power Electronic Conference West 1988, Seminar 501

5.) Modelling, Analysis and Compensation of the Current-Mode Convert, Application Note U-97 by Unitrode

6.) Using the SPICE2 CAD Package to Simulate and Design the Current Mode Converter by Dr. Bello, Proceedings pf Powercon 11, 1984

7.) Modern Control Engineering by K. Ogata, copyright 1990, published by Prentice-Hall Inc.