SECTION 5:

ANALOG DESIGN PRACTICES

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Section 5

ANALOG DESIGN PRACTICES

This section deals with the "how to" portion of analog design.

The objective here is to describe design tools and practices, not to define all the different types of circuits that could be designed. Where needed, examples are used to show the design tool in application.

5.1 ANALOG DESIGN PROCESS

The generic steps used in the design process as described in section 3 will be expanded upon here with regard to analog design. Section 3 should be used as a companion to this subsection since this is not a rigorous description of the design process but how analog design is applied in the design process.

The design task given to an analog circuit designer will usually be described by a specification, detailed circuit description and a detailed block diagram. The task then is to design and verify that the circuit will satisfy these constraints. The first major task is to select the appropriate components and design the circuit so that the design requirements are met. The search for components will ordinarily be constrained by preferred components lists, etc. as outlined in section 10 of this document. The process of choosing the right component involves detailed investigation of all its characteristics. (Component selections are not final until the circuit is built and shown to meet specifications by test. Often several iterations of analyze, build and test are required to reach this point.) The circuit design is analyzed using CAD techniques and/or hand calculations and the exercise of good engineering judgment. Preliminary choices usually follow a process that analyzes each stage individually supplemented by analyses of the overall chain of stages involved in each major function of the design. These analyses must consider the attributes of the parts used.

5.2 ANALOG DESIGN TOOLS

The analog circuit designer should use every resource at his or her disposal to get the job done. Circuit analysis and design resources at ITT-A/OD include PSPICE, IGSPICE and smaller PC-based circuit simulator programs see Table 5.2.1. Some types of circuit designs require using computers (VAX or PC) to perform the analysis. Other types of design can be performed by hand. Whichever approach is used, a check on your analysis and design should be performed.

Table 5.2.1. Analog Circuit Design Tools (Computer Programs)

BOSS	- Block Oriented System Simulation.
ICSSM	- Interactive Communication System Simulation Model Program.
IG-SPICE	- Interactive Graphics general purpose circuit simulation program for nonlinear DC, nonlinear transient, and linear AC analysis.

Table 5.2.1. Analog Circuit Design Tools
(Computer Programs) (Cont.)

MSIMON	- Subset of SPICE transient analysis of MOS digital circuits.
MIDAS	- Modified Integrated Digital Analog Simulator.
SPICE	- This program simulates analog components when timing analysis of a portion of a circuit is more critical.
PSPICE	- This program simulates analog components when timing analysis of a portion of a circuit is more critical.
SCEPTRE	- Non-SPICE based circuit simulator program.
QUICKSIM	- Simulation and timing analysis program. Used for best case and worse case analysis.
M-SPICE	- This program simulates analog components when timing analysis of a portion of a circuit is more critical.
SPP	- Signal Processing Program which analyzes linear and non-linear systems. Based on a 5/2 FFT.
PCPLOT	- High resultion graphics program.
ACTFIL2*	- Active filter synthesis program which can be used for designing filters given the required characteristics.
LCFIL*	- Passive filter synthesis program which can be used for designing filters given the required characteristics.
LOCIPRO*	- Root Locus analysis program.
XFER	- Transfer function analysis program.
TEKCALC*	- Curve-fitting program.
MATRIX MAGIC*	- Matrix manipulation program.
TRANSFORMER SPREADSHEET	- Transformer design program for single phase multi-winding transformers.
INDUCTOR SPREADSHEET	- Inductor design program.
BUCK, T-BUCK, FLYBACK, and BOOST	- Switching regulator analysis program.

*Not presently available.

Table 5.2.1. Analog Circuit Design Tools
(Computer Programs) (Cont.)

3D GRAPHICS*	- 3 dimension plots for Lotus 1-2-3.
HARVARD GRAPHICS	- General purpose software used to make presenta tion material -- graphs, charts, viewgraphs, etc.
PLOT 10	- Tektronic terminal graphical package.
MATHCAD	- Plotting of mathematical computations.
ORCAD	- Schematic capture, partlist & netlist generation, expandable for circuit simulation.
SCIDESIGN	- Schematic Capture with back annotation, partlist and netlist generation, expandable for circuit simulation.
SYSCAP*	- Vax or external service based circuit simulator program. Numerous analytical capabilities to include nuclear effects analysis.
ANALOG WORKBENCH	- PC or Work Statiion based circuit simulator program. Many enhanced circuit analysis functions with test equipment type output displays.
MICRO CAP II & III*	- PC based analog circuit simulator program. Net list extracted automatically from schematic.
PRECISE*	- Enhanced SPICE based analog circuit simulator program.
BIFET	- Semiconductor model parameter generation software. (SPICE)
INCA	- Interactive Control Analysis for system analysis.
NETED/SYMED	- Schematic capture, partlist & netlist generation, for best case and worse case simulation.
STEP	- This utility program converts the simulation results into a functional test pattern file for use on the Sentry.
BASIC	- Higher level language which actually consists of several version.
PASCAL	- Higher level language with several versions.

*Not presently available.

Table 5.2.1. Analog Circuit Design Tools
(Computer Programs) (Cont.)

FORTRAN	- Higher level language a Vax which has numerous subduties available to it (IMSL - STAT/LIBRARY, SFUN/LIBRARY & MATH/LIBRARY)
C	- Higher level language includes Vax and PC versions.

*Not presently available.

There exists numerous type of test equipment which can be used in the test and evaluation of analog circuit designs. Table 5.2.2 contains a list of some of the equipment that could be used by the engineer. The normal types of test equipment such as power supplies, oscilloscopes, digital voltmeters, etc. are not included.

Table 5.2.2. Analog Design Tools
(Test Equipment)

Audio Spectrum Analyzer	- Used to determing frequency response of the circuit under test.
Sound Analysis System	- Used to measure acoustical energy and provide output information.
Audio Analyzer	- Contains both a digitally controlled signal source and digital voltmeter.
Digital Oscilloscope	- Can be used for evaluating low frequency characteristics.
Thermograph	- Used to measure temperature and output the results on a strip chart and display.
Current Probe	- Used to measure current through a line indirectly.
RF Spectrum Analyzer	- Used to determine frequency response of a circuit.
Network Analyzer	- Used in the characterization of circuits and components.

Another important asset available to the circuit designer is data and reference books. Data books are provided by vendors and can be acquired from local vendor representatives. Reference books are available in the ISC in TAC II, from other engineers in your area, or from your own collection. If you use reference books or data books to design circuits, a circuit analysis should still be performed before you commit to the design.

Finally, one of the most important resources is other engineers. Design reviews and conversations with other engineers will provide you with valuable information regarding your circuit.

5.3 DC ANALYSIS

This subsection describes specific application, techniques, and technologies in analog design relative to DC analysis.

5.3.1 DC Offset and Bias Selection

DC offset bias selection is an important step in the design and analysis of a circuit. Two examples will be used to show the importance of these two items.

First, proper dc biasing of a transistor stage helps prevent instability and nonlinear response to ac waveforms. Usually, the operating point can be selected from the "V_{ce}/I_c" plot for the transistor; see Figure 5.3.1-2.

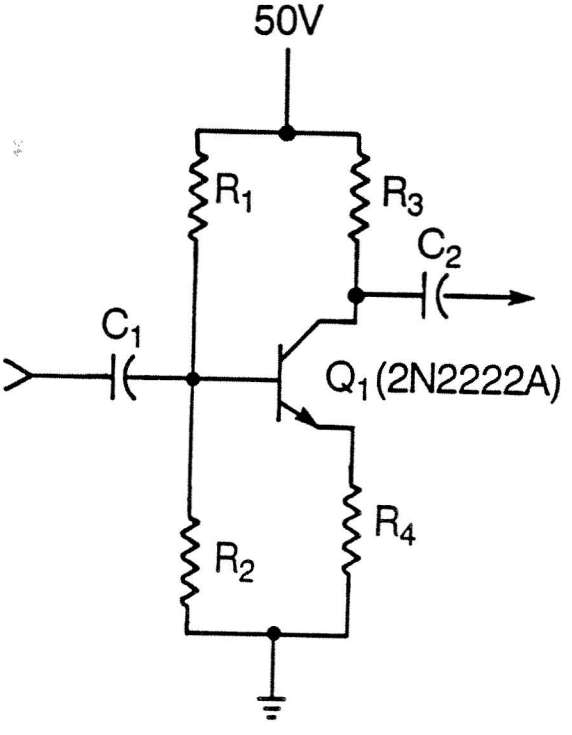


Figure 5.3.1-1.
CE Self-Bias Transistor

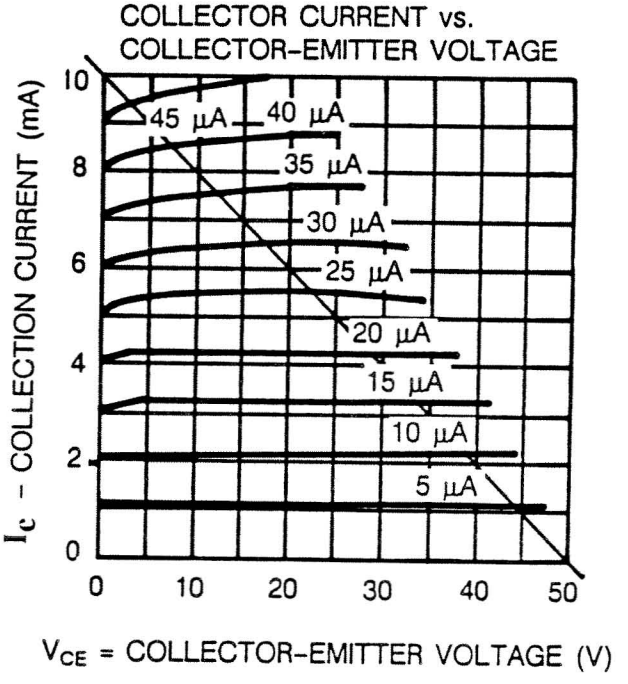


Figure 5.3.1-2.
V_{ce} VS I_c

The "load line" is established as a line between the V_{ce} voltage where the transistor is "off" and the I_c current where the transistor is full "on." To establish an operation point and thus dc bias for the transistor, an operation point for the circuit in Figure 5.3.1-1 is selected from Figure 5.3.1-2 as:

$$I_b = 23\ \mu a, \qquad \text{(Eq. 5.3.1-1)}$$

$$V_{ce} = 25 \text{ volts}, \qquad \text{(Eq. 5.3.1-2)}$$

$$I_c = 5 \text{ ma} \qquad \text{(Eq. 5.3.1-3)}$$

and

$$h_{FE} = I_c/I_b = 217. \qquad \text{(Eq. 5.2.1-4)}$$

(A dc current gain h_{FE} of 217 is not uncommon for a transistor.) Next, it is necessary to determine the emitter resistor, R_4, value if the collector resistor, R_3, is selected to be equal to 1 Kohm. Thus,

$$V_{ce} = V_{CC} - (I_cR_s + [I_b + I_c]R_4) \qquad \text{(Eq. 5.3.1-5)}$$

or

$$25.0 \text{ Vdc} = -(5\text{ma})(1\text{K}\Omega) + 50 \text{ Vdc} - (23\text{ua} + 5\text{ma})R_4 \qquad \text{(Eq. 5.3.1-6)}$$

or

$$R_4 \simeq 4.0 \text{ Kohms}\Omega. \qquad \text{(Eq. 5.3.1-7)}$$

For a transistor to operate in the active region, its base-to-emitter junction must be forward biased and its base-to-collector junction must be reverse biased. The collector voltage, V_c, is equal to

$$V_c = V_{CC} - I_cR_3 \qquad \text{(Eq. 5.3.1-8)}$$

or

$$V_c = 50 \text{ Vdc} - (5\text{ma})(1\text{K}) = 45 \text{ Vdc}. \qquad \text{(Eq. 5.3.1-9}$$

The emitter voltage, V_e, is equal to

$$V_e = V_{CC} - V_c - (I_b + I_c)R_4 \qquad \text{(Eq. 5.3.1-10)}$$

or

$$V_e = (I_b + I_c)R_4 \qquad \text{(Eq. 5.3.1-11)}$$

or

$$V_e = (23\text{ua} + 5\text{ma})4.0\text{K}\Omega = 20.0 \text{ Vdc} \qquad \text{(Eq. 5.3.1-12)}$$

and for a silicon transistor an additional 0.7 volts will be added to forward bias the base to emitter junction. Therefore, the base voltage must be

$$V_b = V_e + 0.7 = 20.7 \text{ Vdc}. \qquad \text{(Eq. 5.3.1-13)}$$

The load line and equations 5.3.1-1 and 5.3.1-2 show that 23 uA of base current is required to turn on the transistor. As a rule of thumb, the current through R_1 should be 50 times the required I_b. The value for R_1 and R_2 can now be determined:

$$R_1 = \left(\frac{50 \text{ V} - 20.7 \text{ V}}{50\ (23\text{uA})}\right) = 25.5 \text{ Kohm} \qquad \text{(Equation 5.3.1-14)}$$

and

$$R_2 = \left(\frac{20.7 \text{ V}}{(50 - 1)\ (23\text{uA})}\right) = 18.4 \text{ Kohm} \qquad \text{(Equation 5.3.1-15)}$$

Nonetheless, numerous specifications could still be addressed such as: stability, frequency response, linearity, dynamic range, etc. This analysis should be considered a first order approximation to DC biasing only.

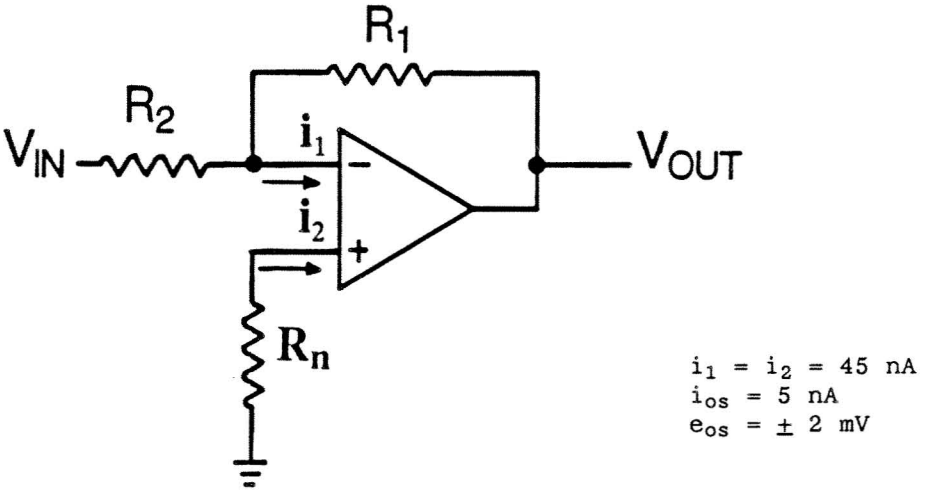


Figure 5.3.1-3. Inverting Op-Amp Stage

Another example to consider is the dc compensation technique for inverting op-amp stages. The method is to add a resistance from the noninverted input of the op-amp to ground which is equal to the Thevenin equivalent dc resistance as seen from the inverting side of the op-amp. The purpose of the dc compensation is actually due to the dc offset introduced by input bias currents, i_1 and i_2. If R_n in Figure 5.3.1-3 is not included, the dc offset due to the input bias currents and input offset voltage is

$$V_0 = \frac{(R_1 + R_2)\ ((R_1 \,//\, R_2) i_1 + e_{os})}{R_2} = 22.45\text{mv} \qquad \text{(Eq. 5.3.1.16)}$$

where

$R_1 = 10\text{K}\Omega$, (Eq. 5.3.1-17)

$R_2 = 1\text{K}\Omega$, (Eq. 5.3.1-18)

$i_1 = 45\eta\text{a}$ (Eq. 5.3.1-19)

and

$e_{os} = 2\text{mv}$. (Eq. 5.3.1-20)

With R_n in the circuit the output voltage, Vo, due to the input bias current and input offset voltage is

$$V_O = \frac{(R_1 + R_2)\ ((R_1 \,//\, R_2) i_{os} + e_{os})}{R_2} = 22.05mv \qquad \text{(Eq. 5.3.1.21)}$$

where

$R_1 = 10K\Omega,$ (Eq. 5.3.1-22)

$R_2 = 1K\Omega,$ (Eq. 5.3.1-23)

$i_{os} = 5\eta a$ (Eq. 5.3.1-24)

and

$e_{os} = 2mv.$ (Eq. 5.3.1-25)

This would require

$$R_n = R_1 \,//\, R_2 = 9.091K\Omega. \qquad \text{(Eq. 5.3.1-26)}$$

Further dc offset compensation could be performed by connecting R_n to a variable voltage which could be adjusted to cancel the input offset voltage.

5.3.2 DC Gain

The dc gain of a circuit is determined at zero Hz. In transistors, this gain may be the dc current gain "B" or "h_{FE}." This gain should not be confused with the "h_{fe}" or small signal current gain. At dc, capacitors are treated like "opens" and inductors are treated like "shorts." From a transfer function standpoint, the transfer function can be rationalized and replaced by

$$H(s) \rightarrow \text{Real } H(j\omega) \pm j \text{ Imaginary } H(j\omega) \qquad \text{(Eq. 5.3.2-1)}$$

and

$$\text{Real } H(j\omega)\Big|_{\omega = 0} = H(j\omega) \text{ @ dc} \qquad \text{(Eq. 5.3.2-2)}$$

or in simpler terms

$$H(s)\Big|_{s = 0} = H(s) \text{ @ dc.} \qquad \text{(Eq.a 5.3.2-3)}$$

DC gain should not be confused with the Final-Value theorem:

$$\lim_{t \to \infty} h(t) = \lim_{s \to 0} sH(s) \qquad \text{(Eq.a 5.3.2-4)}$$

which deals with the response of a circuit or system.

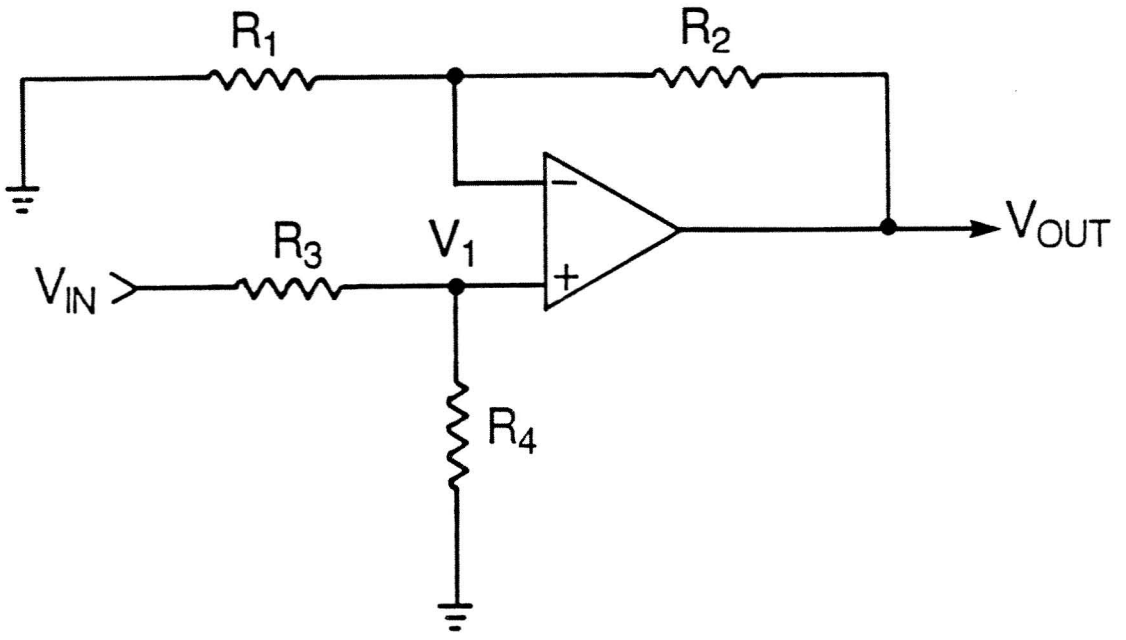


Figure 5.3.2-1. Example Circuit

As an example of calculating the dc gain of a circuit, the circuit in Figure 5.3.2-1 will be analyzed. The voltage at the noninverted input of the op-amp, V_1, is determined by using the voltage divider rule between R_3 and R_4 or

$$V_1 = \frac{(Vin)(R_4)}{R_3 + R_4} \cdot \qquad \text{(Eq. 5.3.2-5)}$$

Next, using Kirchhoff's Current Law, the current through R_1 is equal to the current through R_2 or

$$\frac{V_1}{R_1} = \frac{Vout - V_1}{R_2} \qquad \text{(Eq. 5.3.2-6)}$$

or

$$\frac{Vout}{V_1} = 1 + \frac{R_2}{R_1} \cdot \qquad \text{(Eq. 5.3.2-7)}$$

Thus, the overall dc gain would be

$$\frac{Vout}{Vin} = \left[\frac{R_4}{R_3 + R_4}\right]\left[1 + \frac{R_2}{R_1}\right] . \qquad \text{(Eq. 5.3.2-8)}$$

5.3.3 DC Sensitivity Analysis

DC sensitivity analysis has gained in popularity because various circuit simulator programs lack the ability to perform ac sensitivity analysis. In the dc mode, the frequency-related terms are nulled (to correctly null pole/zero cancellation must also result in gain modification) and the sensitivity is determined. An example circuit is provided in Figure 5.3.3-1.

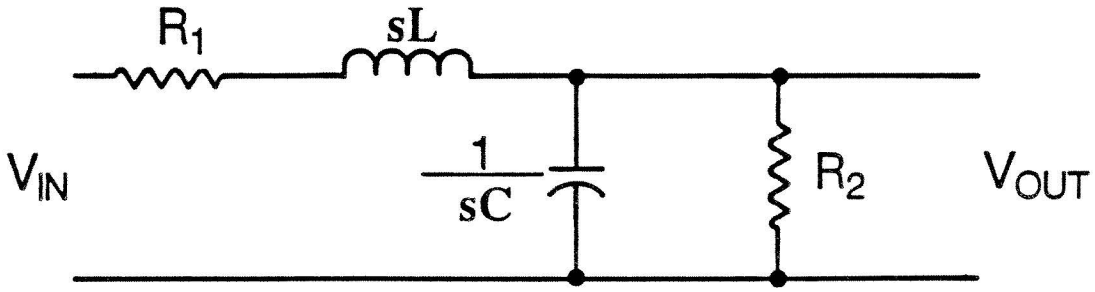


Figure 5.3.3-1. DC Circuit Example

The transfer function for the example circuit is

$$\frac{Vout}{Vin} = \frac{R_2}{s^2\,LCR_2 + s(CR_1R_2 + L) + R_1 + R_2} \quad \text{(Eq. 5.3.3-1)}$$

Next, the transfer function is rationalized into its real and imaginary parts and coefficients are substituted for with constants or

$$\left|\frac{Vout}{Vin}\right| = \frac{(A)}{((D-B\omega^2) + j\omega C)} \quad \frac{((D-Bw^2) - jwC)}{((D-B\omega^2) - j\omega C)} \quad \text{(Eq. 5.3.3-2)}$$

$$s \rightarrow j\omega$$

or

$$\frac{Vout}{Vin} = \frac{A(D - B\omega^2)}{(D - B\omega^2)^2 + (j\omega C)^2} - \frac{j\omega AC}{(D - B\omega^2)^2 + (j\omega C)^2} \quad \text{(Eq. 5.3.3-3)}$$

For a dc sensitivity analysis the frequency term ω is equal to zero. Thus, the transfer function becomes

$$\left.\frac{Vout}{Vin}\right| = \frac{A}{D} = \frac{R_2}{R_1 + R_2} \quad . \qquad \text{(Eq. 5.2.3-4)}$$

$$\omega = o$$

The dc sensitivity relative to R_2 becomes

$$S^{DC}_{R_1} = \frac{R_1 + R_2 - R_2}{(R_1 + R_2)^2} = \frac{R_1}{(R_1 + R_2)^2} \qquad \text{(Eq. 5.3.3-5)}$$

and due to R_1

$$S^{DC}_{R_1} = \frac{-R_2}{(R_1 + R_2)^2} \quad . \qquad \text{(Eq. 5.3.3-6)}$$

If

$$R_1 = R_2 = 1$$

then the corresponding dc sensitivities are

$$S^{DC}_{R_2} = 0.25 \qquad \text{(Eq. 5.3.3-7)}$$

and

$$S^{DC}_{R_1} = -0.25. \qquad \text{(Eq. 5.3.3-8)}$$

A sensitivity which is less than ± 1 implies that variations in either of the resistors, R_1 or R_2, has little impact on the dc response.

5.3.4 Other DC Tools (Pole/Zero Cancellation)

Pole/zero cancellation can be used to simplify a high order transfer function. Typically, poles and zeros can be cancelled with the modification of the gain. For example, suppose the following transfer function is considered:

$$\frac{Vout}{Vin} = \frac{10(s + 30)}{(s + 20)(s + 50)} \quad . \qquad \text{(Eq. 5.3.4-9)}$$

The highest frequency pole or zero is the pole at 50 rads/sec. It can be cancelled by dividing the gain by the pole or

$$\frac{Vout}{Vin} = \frac{(10/50)(s + 30)}{(s + 20)} \quad . \qquad \text{(Eq. 5.3.4-2)}$$

Next, the zero at 30 rads/sec can be cancelled by multiplying the gain by 30 or

$$\frac{Vout}{Vin} = \frac{(0.2)(30)}{(s + 20)} \quad . \qquad \text{(Eq. 5.3.4-3)}$$

The final pole can be cancelled to produce the dc gain of

$$\frac{Vout}{Vin} = \frac{6}{20} = 0.3 \ . \qquad \text{(Eq. 5.3.4-4)}$$

The same 0.3 results would occur if in Equation 5.3.4-1 the "s" term was zeroed initially.

5.4 AC ANALYSIS

This section describes specific applications, techniques, and technologies in AC circuit design and analysis.

5.4.1 AC Gain, Bandwidth and Bode Plots

The ac frequency response is an essential analytical tool. The conventional Bode plot is used to show the relationship between gain (measured in decibels) and phase (measured in degrees). Circuit stability can be directly determined based on the gain/phase relationship. Usually, the "x" axis of the Bode plot is a log scale. Hence, 20 dB per decade or 6 dB per octave can be readily determined.

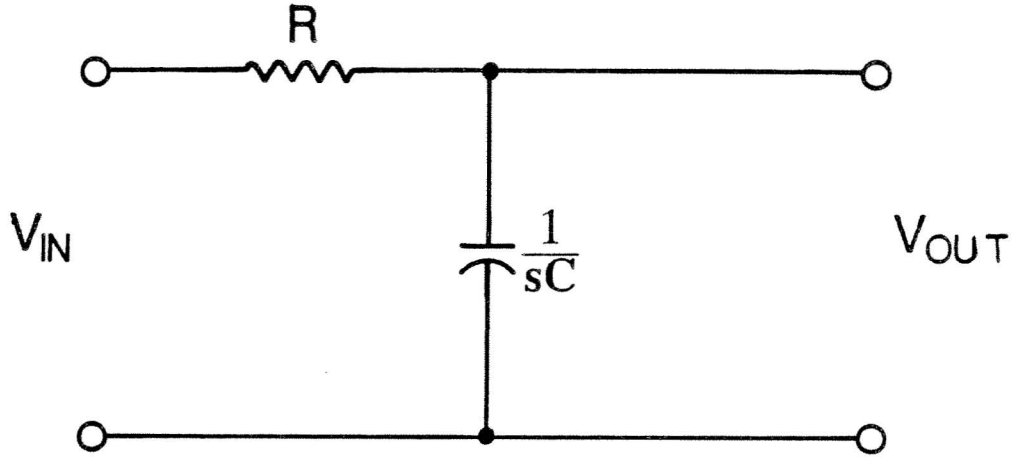


Figure 5.4.1-1. Low Pass Circuit

As an example of ac frequency response, the following simple low pass will be analyzed. Assume a simple low pass circuit as shown in Figure 5.4.1-1. The transfer function for the circuit is

$$Z(s) = \frac{1/RC}{s + 1/RC} \quad . \qquad \text{(Eq. 5.4.1-1)}$$

Several points of interest can be directly determined from the transfer function. First, there is a pole at 1/RC with no zeros present. Second, the dc gain would be

$$\left.\frac{Vout}{Vin}\right|_{s = 0} = \frac{1/RC}{0 + 1/RC} = 1 = 0 \text{ dB} \quad . \qquad \text{(Eq. 5.4.1-2)}$$

A Bode plot can be drawn from the rationalized transfer function. A rationalized transfer function separates the real and imaginary portion of the transfer function by multiplication of the denominator's complex conjugate pair. Thus, Equation 5.4.1-1 becomes

$$Z(j\omega) = \left.\frac{Vout}{Vin}\right|_{j\omega \rightarrow s} = \frac{1/RC}{j\omega + 1/RC} \; \frac{(1/RC - j\omega)}{(1/RC - j\omega)} \qquad \text{(Eq. 5.4.1-2)}$$

or

$$Z(j\omega) = \frac{(1/RC)^2}{\omega^2 + (1/RC)^2} - j \frac{\omega/RC}{\omega^2 + (1/RC)^2} \qquad \text{(Eq. 5.4.1-4)}$$

where

$$Re(j\omega) = \frac{(1/RC)^2}{\omega^2 + (1/RC)^2} \qquad \text{(Eq. 5.4.1-5)}$$

and

$$Im(j\omega) = \frac{-\omega/RC}{\omega^2 + (1/RC)^2} \qquad \text{(Eq. 5.4.1-6)}$$

or

$$Mag(j\omega) = \{Re(j\omega)^2 + Im(j\omega)^2\}^{1/2} \qquad \text{(Eq. 5.4.1-7)}$$

and

$$\phi(j\omega) = \tan^{-1} (Im(j\omega)/Re(j\omega)), \qquad \text{(Eq. 5.4.1-8)}$$

Let

$$R = 1K\Omega \qquad \text{(Eq. 5.4.1-9)}$$

and

$$C = 1uf. \qquad \text{(Eq. 5.4.1-10)}$$

Next determine the gain phase plot using Equations 5.4.1-7 and 5.4.1-8 and the component values for "R" and "C".

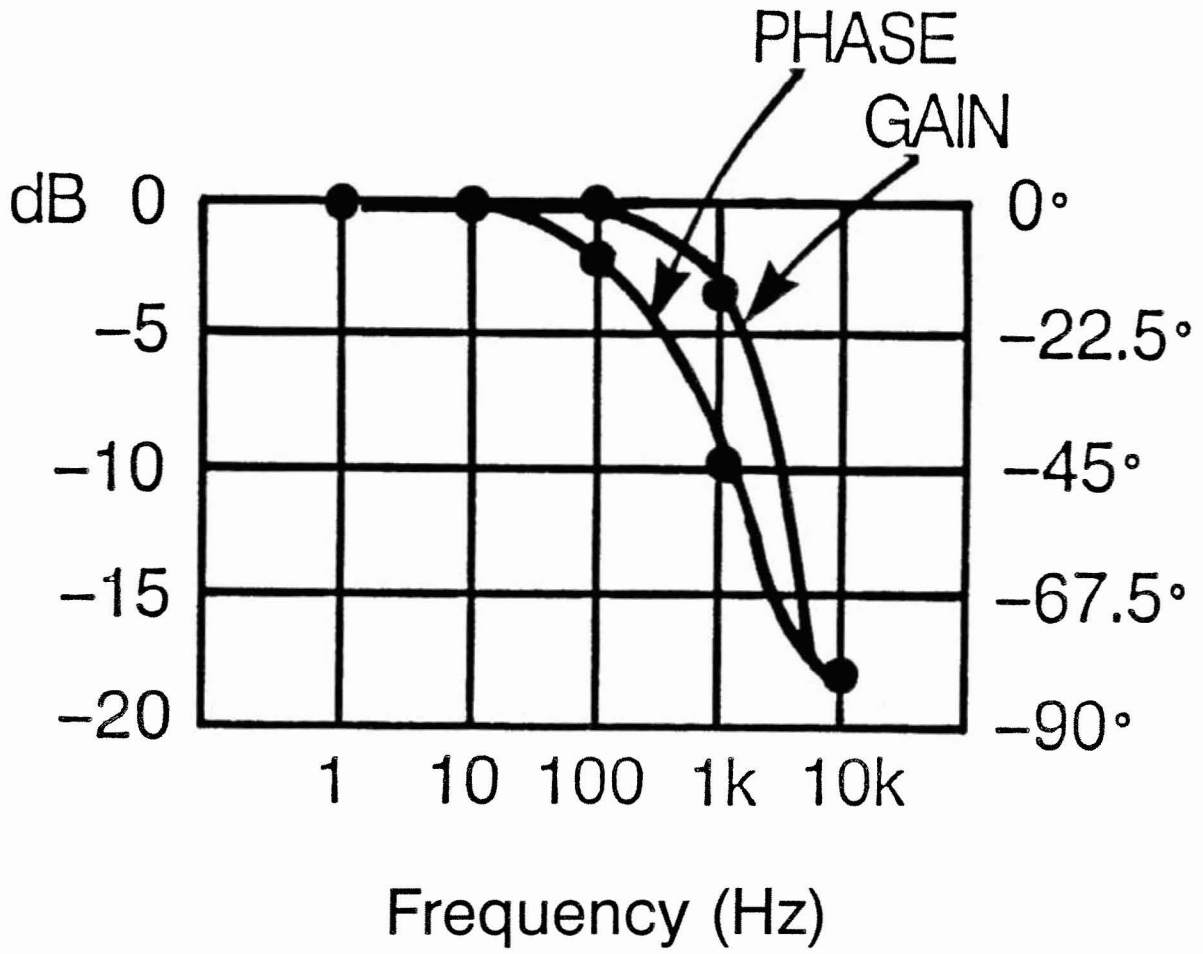


Figure 5.4.1-2. Bode Plot

From the Bode plot, Figure 5.4.1-2, the low pass filter has a -3 dB point at 1K rads/sec and a phase shift of -45°. The dc or low frequency gain is 0 dB with a -20 dB/decade roll off at 1Krad/sec. Since the gain never gets above 0 dB, it is an unconditionally stable, and the phase shift never exceeds -90°.

5.4.2 Phase and Frequency Compensation

Many times, it is necessary to add phase or frequency compensation to a circuit to improve its stability or limit the excursions of its transient response.

Phase or gain compensation is usually added to improve the stability of a circuit. Gain compensation is the easiest way to improve stability because the phase is usually unaffected by gain shifts. The problem with this approach is that low frequency gain is lost in this process. Another method of compensating a circuit is to add phase compensation in the form of lead/lag compensation. This consists of adding a low frequency zero and high frequency pole which straddle the crossover point.

As an example of both of these compensation approaches, a circuit with the transfer function of

$$\frac{Vo(s)}{Vin(s)} = \frac{80E3}{s(s+20)(s+50)} = \frac{80E3}{s^3 + 70s^2 + 1000S} \qquad \text{(Eq. 5.4.2-1)}$$

will be evaluated. First, the transfer function can be rationalized and becomes

$$\frac{Vo(j\omega)}{Vin(j\omega)} = \frac{80E3}{-70\omega^2 + j(1000\omega - \omega^3)} \qquad \text{(Eq. 5.4.2-2)}$$

or

$$\frac{Vo(j\omega)}{Vin(j\omega)} = \frac{-5.6E6\omega 2}{4900\omega^4 + (1000\omega - \omega^3)^2} - j\,\frac{80E3(1000\omega - \omega 3)}{4900\omega^4 + (1000\omega - \omega^3)^2} . \qquad \text{(Eq. 5.4.2-3)}$$

The real portion of Equation 5.3.2-3 is

$$Re(j\omega) = \frac{80E3}{4900\omega^4 + (1000\omega - \omega^3)^2} \qquad \text{(Eq. 5.4.2-4)}$$

and imaginary portion is

$$Im\ (j\omega) = \frac{-80E3(1000\omega - \omega^3)}{4900\omega^4 + (1000\omega - \omega^3)^2} . \qquad \text{(Eq. 5.4.2-5)}$$

This can be expressed as magnitude, $M(j\omega)$, and phase, $\phi(\omega)$ as

$$M(j\omega) = 20 \log \{Re(j\omega)^2 + Im\ (j\omega)^2\}^{1/2} \qquad \text{(Eq. 5.4.2-6)}$$

and

$$\phi(j\omega) = \tan^{-1}\ (Im(j\omega)/Re(j\omega)) . \qquad \text{(Eq. 5.4.2-7)}$$

Table 5.4.2-1. Frequency Response

	Uncompensated		Gain Compensated		Phase Compensated	
ω	M(jω)	Φ(jω)	M(jω)	Φ(iω)	M(jω)	Φ(iω)
1	38 dB	-94°	36 dB	-94°	38 dB	-92°
2	32 dB	-98°	30 dB	-98°	32 dB	-94°
5	24 dB	-109.8°	22 dB	-109.8°	24 dB	-99.9°
10	17 dB	-127.9°	15 dB	-127.9°	17.6 dB	-108.9°
15	12.3 dB	-143.6°	10.3 dB	-143.6°	13.5 dB	-116.9°
20	8.4 dB	-156.8°	6.4 dB	-156.8°	10.5 dB	-123.9°
30	2.1 dB	-177.3°	0.1 dB	-177.3°	5.8 dB	-135.6°
40	-3.2 dB	-192.1°	-5.2 dB	-192.1°	2.2 dB	-145.4°
50	-7.5 dB	-203.2°	-9.5 dB	-203.2°	-0.8 dB	-153.8°
60	-11.4 dB	-211.8°	-13.4 dB	-211.8°	-3.5 dB	-161.1°
70	-14.8 dB	-218.5°	-16.8 dB	-218.5°	-5.8 dB	-167.5°
80	-17.8 dB	-224°	-19.8 dB	-224°	-8.0 dB	-173.1°
90	-20.6 dB	-228.4°	-22.6 dB	-228.4°	-9.9 dB	-178.2°
100	-22.9 dB	-232.1°	-24.9 dB	-232.1°	-11.7 dB	-182.7°

The uncompensated frequency response is listed in Table 5.4.2-1. Plotting the phase and gain of the uncompensated response (Bode Plot) shows that the existing transfer function would result in an unstable response; see Figure 5.4.2-1. Either a gain or phase compensation is required to assure stability. If the dc gain is reduced by 2 dB, the phase shift at crossover will be less than 180°. This would correspond to gain compensation. With gain compensation, the phase response does not change; see Table 5.4.2-1 and Figure 5.4.2-1. The major drawback to gain compensation is the low frequency gain reduction and reduced bandwidth. Another type of compensation, phase compensation, adds phase at crossover without reducing the low frequency zero and high frequency pole around the crossover point. In this case, crossover is about 33 Hz. A lead/lag network of

$$C(s) = \frac{8(s+25)}{s + 200} \qquad \text{(Eq. 5.4.2-8)}$$

will be used to compensate Equation 5.3.2-1. Therefore, the new transfer function becomes

$$\frac{Vout(s)}{Vin(s)} = \frac{6.4E5(s + 25)}{s^4 + 270s^3 + 15E3s^2 + 2E5s} \qquad \text{(Eq. 5.4.2-9)}$$

Rationalized and conjugated into its real and imaginary parts Equation 5.4.2-4 becomes

$$Re(j\omega) = \frac{6.4E5(-245\omega^4 + 21.25E5\omega^2)}{(\omega^4 - 15E3\omega^2)^2 + (2E5\omega - 270\omega^3)^2} \qquad \text{(Eq. 5.4.2-4)}$$

and

$$Im(jw) = \frac{6.4E5(w^5 - 8.25E3w^3 - 6.25E7w)}{(w^4 - 15E3w^2)^2 + (2E5w - 270w^3)^2} . \qquad \text{(Eq. 5.4.2-11)}$$

As can be seen from Table 5.4.2-1 and Figure 5.4.2-1, the phase at crossover for the phase compensated circuit is less than 180^0. Therefore, the circuit is stabilized. Phase compensation in this approach would add components and increase the crossover frequency from 34 to 46 rad/sec.

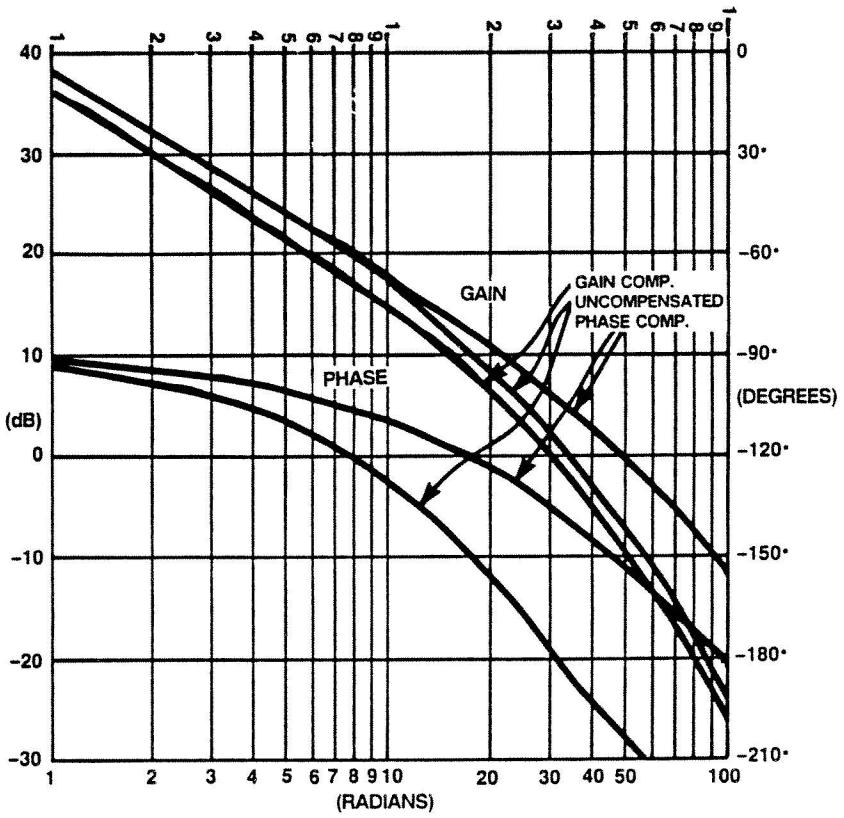


Figure 5.4.2-1. Bode Plot

5.4.3 Oscillations, Resonant Peaks and Stability

The stability of a circuit can be determined by using several techniques. The Roth-Hurwitz Stability Criterion, Nyquist plots, Bode plots or evaluation of the pole location in the characteristic equation can all be used. In simple terms, an oscillator is produced when there is more than 180^0 of phase shift and more than 0 dB of gain in the open loop response, $G(j\omega)H(j\omega)$.

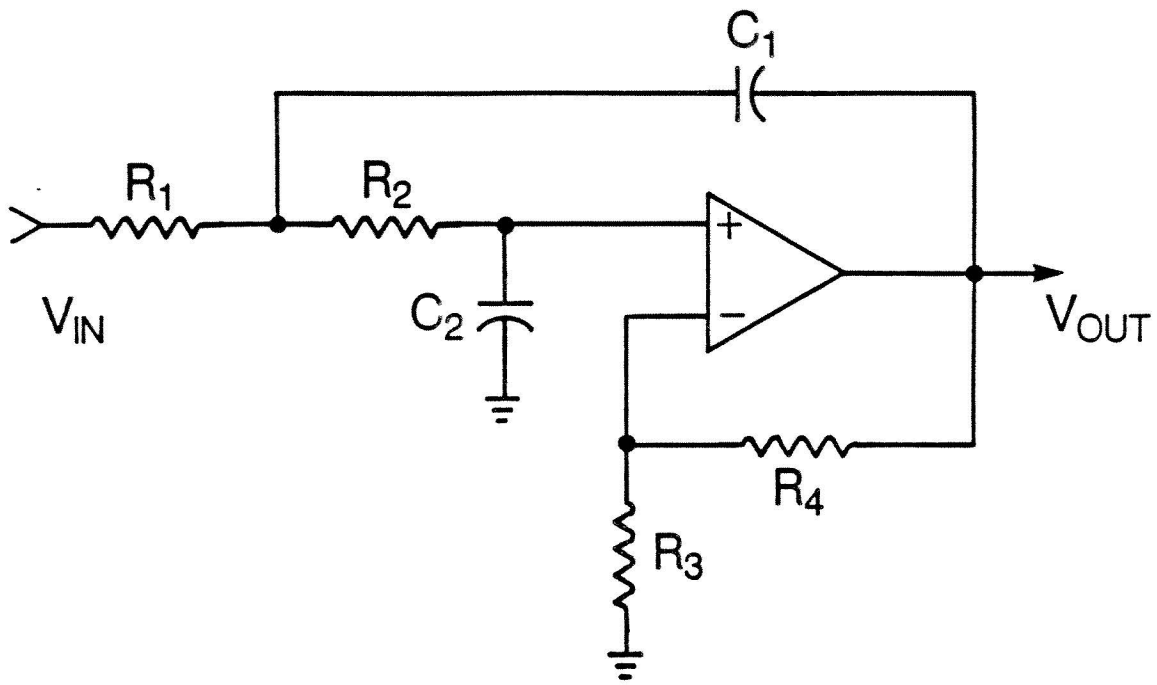


Figure 5.4.3-1. Example Circuit

To illustrate how a circuit could be usable the Sallen-Key low pass active filter is provided as an example circuit.

The dc gain of the example circuit is determined by the relationship between R_3 and R_4 or

$$K = 1 + R_4/R_3 \qquad \text{(Eq. 5.4.3-1)}$$

and the overall transfer function for Vout/Vin becomes

(Eq. 5.4.3-2)

$$\frac{Vout}{Vin} = \frac{K/R_1R_2C_1C_2}{s^2 + (1/RC_1C_1 + 1/R_2C_1 + 1/R_2C_2 - K/R_2C_2)s + 1/R_1R_2C_1C_2}$$

If

$$R_1=R_2=C_1=C_2=1 \qquad \text{(Eq. 5.4.3-3)}$$

then the transfer function can be reduced to

$$\frac{Vout}{Vin} = \frac{K}{s^2 + (3 - K)s + 1} \quad . \qquad \text{(Eq. 5.4.3-4)}$$

As "K" increases in value the coefficient of "s" gets smaller. When "K" is equal to three the coefficient of "s" is equal to zero. The inverse Laplace transform of Equation 5.3.3-4 if "K" is equal to three is

$$L^{-1}\left\{\frac{(3)}{(s^2 + 1^2)}\right\} = 3\mathrm{Sin}(t) \ . \qquad \text{(Eq. 5.4.3-5)}$$

Equation 5.4.3-5, shows that oscillations would occur if "K" is equal to three. Thus, the circuit is unstable.

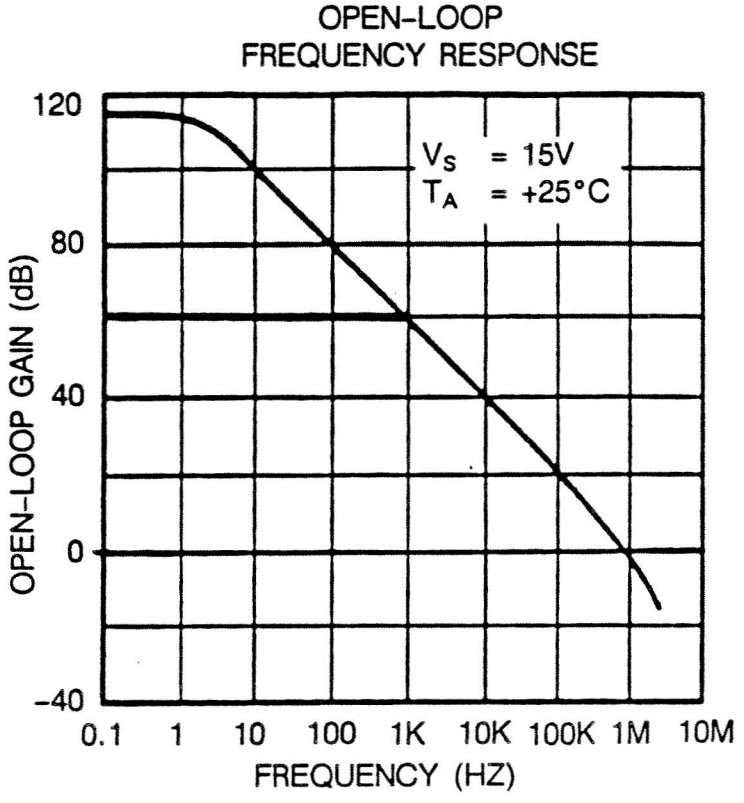


Figure 5.4.3-2.
Open Loop Response

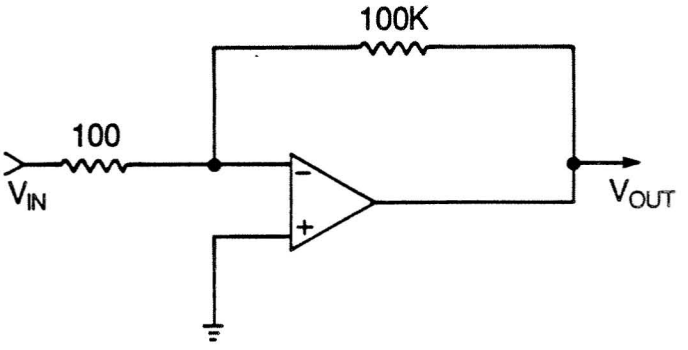


Figure 5.4.3-3.
Example Circuit

The open loop frequency response of an op-amp defines the limits of both the dc gain and crossover frequency for a circuit performance. Suppose the voltage gain of Figure 5.4.3-3 is.

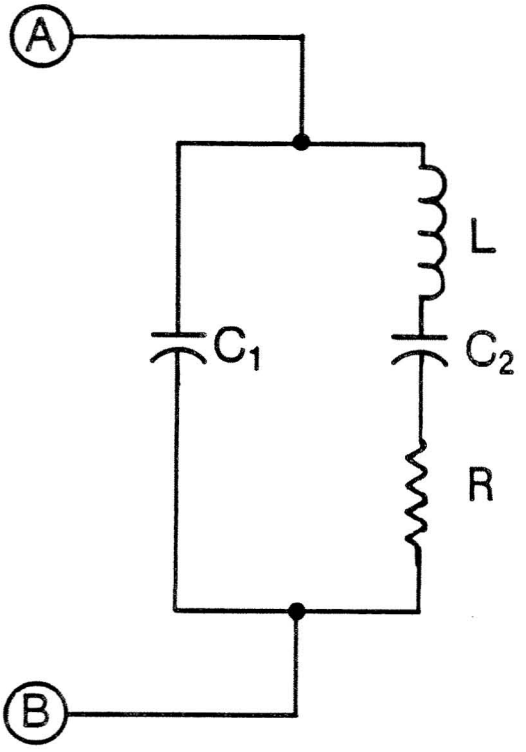
$$\frac{Vout}{Vin} = \frac{100K}{100} = 60 \text{ dB} \ . \qquad \text{(Eq. 5.4.3-6)}$$

This translates into the open loop frequency response shown in Figure 5.4.3-2. The low frequency pole that was at 1 Hz due to the op-amp moves to 1 kHz. In addition, if reactive components result in poles and zeros beyond the 1 kHz pole, the additional poles or zeros will be restricted to cause the performance of the circuit to be bound by the open loop response of the op-amp.

It should be noted before leaving this section that resonant peaks cause their own set of problems. Many times a resonant peak can produce an unstable condition if the input signal strength is strong enough to cause saturation of amplifiers. In servo loops this is referred to as saturation oscillation. In addition, resonant peaks can and do distort audio characteristics.

5.4.4 AC Power Calculations

There are several ways to look at ac power calculations relative to complex impedances. Phasors could be used and graphically manipulated to illustrate ac power. However, another approach is to deal with the actual individual components impedances to determine the ac power. First, it is necessary to determine the complex impedance.



C_1 = 1.3 uf
C_2 = 0.26 uf
L = 0.44H
R = 200Ω
F = 1 kHz
Irms = 63.4 mArms

Figure 5.4.4-1. Complex Impedance

For the example circuit in Figure 5.4.4-1

$$Z_1 = 1/sC_1 \qquad \text{(Eq. 5.4.4-1)}$$

and

$$Z_2 = Ls + 1/sC_2 + R \qquad \text{(Eq. 5.4.4-2)}$$

or

$$Z_2 = \frac{s^2(LC_2) + sRC_2 + 1}{sC_2} \qquad \text{(Eq. 5.4.4-3)}$$

and the total admittance, Y_T, is

$$Y_T = sC_1 + \frac{sC_2}{s^2LC_2 + sRC_2 + 1} \qquad \text{(Eq. 5.4.4-4)}$$

or

$$Y^T = \frac{s^3LC_1C_2 + s^2RC_1C_2 + s(C1 + C2)}{s^2LC_2 + sRC_2 + 1} \qquad \text{(Eq. 5.4.4-5)}$$

or the total impedance is equal to

$$Z_T(s) = \frac{s^2LC_2 + sRC_2 + 1}{s^3LC_1C_2 + s^2RC_1C_2 + s(C1 + C2)} \; . \qquad \text{(Eq. 5.4.4-6)}$$

Next, it is necessary to evaluate $Z_T(s)$ at a specific frequency, f. This will require the substitution $j\omega$ into Equation 5.4.4-4 for s. Thus, rewriting Equation 5.4.4-4 to include the "$j\omega$" substitution produces

$$Z_T(j\omega) = \frac{-\omega^2LC_2 + j\omega RC_2 + 1}{-(\omega^2RC_1C_2) + j(\omega C_1 + \omega C_2 - \omega^3LC_1C_2)} \qquad \text{(Eq. 5.4.4-7)}$$

where

$$j^2 = -1 \qquad \text{(Eq. 5.4.4-8)}$$

and

$$j^3 = -j \; . \qquad \text{(Eq. 5.4.4-9)}$$

If the values for ω, C_1, C_2, R and L are substituted into Equation 5.4.4-6, the resulting equation is

$$Z_T(j\omega)\Big|_{f = 1\ kHz} = \frac{-3.51633 + j0.32676}{-0.0026687 - j0.0270883} \qquad \text{(Eq. 5.4.4-10)}$$

or

$$Z_T(j\omega) = 129.75 \ \angle\ 270.3^0 \qquad \text{(Eq. 5.4.4-11)}$$

or

$$Z_T(j\omega) = 0.719 - j129.74. \qquad \text{(Eq. 5.4.4-12)}$$

If the current, Irms, supplied to the complex impedance has an rms magnitude of 63.4 mArms at 1 kHz, then the real portion of the complex power will be equal to

$$Pav = (Irms^2)(Re(Z_T(jw)) = 2.73\ mWatts \qquad \text{(Eq. 5.4.4-13}$$

and the reactive portion of the complex power will be equal to

$$Q = (Irms^2)(Im(Z_T(jw)) = -0.5212\ VARS. \qquad \text{(Eq. 5.4.4-14)}$$

Thus, the complex power expressed in VA (volt-amps) is

$$|S| = \{Pav^2 + Q^2\}^{1/2} = 0.5215\ VA. \qquad \text{(Eq. 5.4.4-15)}$$

5.4.5 Noise Evaluation

Noise in an electronic circuit is due to either external or internal sources. Internal sources of noise are caused by the operation of the electronics in different environments. For example, thermal noise or "Johnson" noise is temperature-dependent and is equal to

$$V_t = \{4KTBR\}^{1/2} . \qquad \text{(Eq. 5.4.5-1)}$$

Where "K" is Bolltzmann's constant (1.38E-23 Joules/degree Kelvin), "T" is temperature expressed in Kelvin, "B" is the noise bandwidth and R is resistance in ohms. Thermal noise is Gaussian and has a mean value of zero volts.

Shot noise is basically caused by variations in current flow across a potential barrier. This type of noise is defined by the equation

$$I_{sh} = \{2QIB\}^{1/2} . \qquad \text{(Eq. 5.4.5-2)}$$

Where "Q" is the electron charge of 1.6e-19 coulombs, "I" is the average dc current and "B" is again the noise bandwidth. Shot noise is also Gaussian.

Contact or "flicker" noise is also an internal noise and is caused by the imperfect junction between two materials. Contact noise is defined by the equation

$$I_f = \frac{GI(B)^{1/2}}{(f)^{1/2}} \cdot \qquad \text{(Eq. 5.4.5-3)}$$

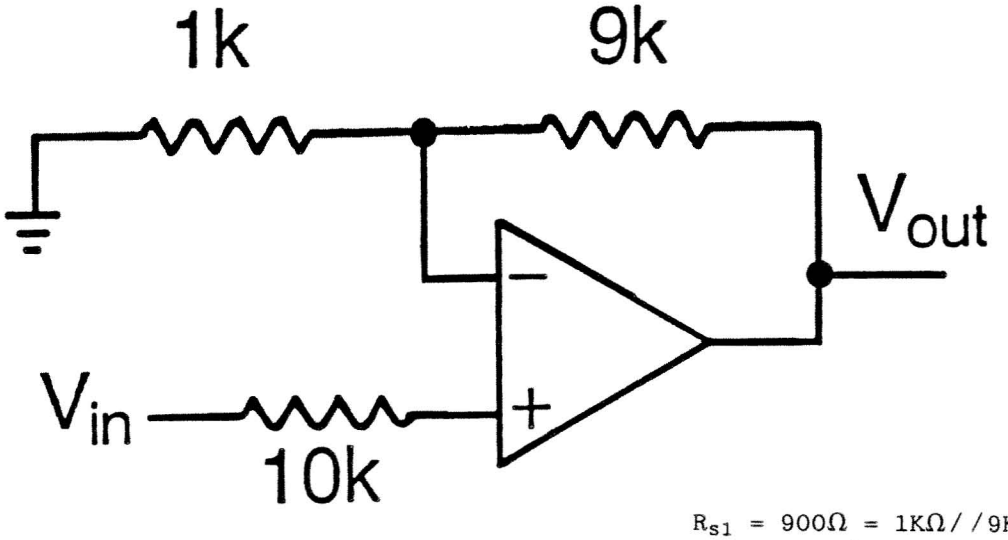
Where "I" is still the average dc current, "B" is still the noise bandwidth; "G" is a constant that is based on the type and material of the contact, and "f" is frequency. In addition, contact noise is Gaussian.

Popcorn noise is typically caused by semiconductor defects. Its magnitude can be between two to 100 times the thermal noise. Usually, this type of noise can be minimized by selecting low noise parts.

The total noise voltage to uncorrelated internal noise sources is expressed as

$$V_T = \{V_t^2 + (I_{SH} + R_{s1})^2 + (I_f R_{s2})^2\}^{1/2} \cdot \qquad \text{(Eq. 5.4.5-4)}$$

As an example of how to calculate the total RMS noise value, suppose the bandwidth of interest is from 0.1 Hz (fl) to 100 Hz (fh). There are in Figure 5.4.5-1 two thermal noise sources, Rs_1 and Rs_2.



$R_{s1} = 900\Omega = 1K\Omega // 9K\Omega$
$R_{s2} = 10\ K\Omega$

Figure 5.4.5-1. Example Circuit

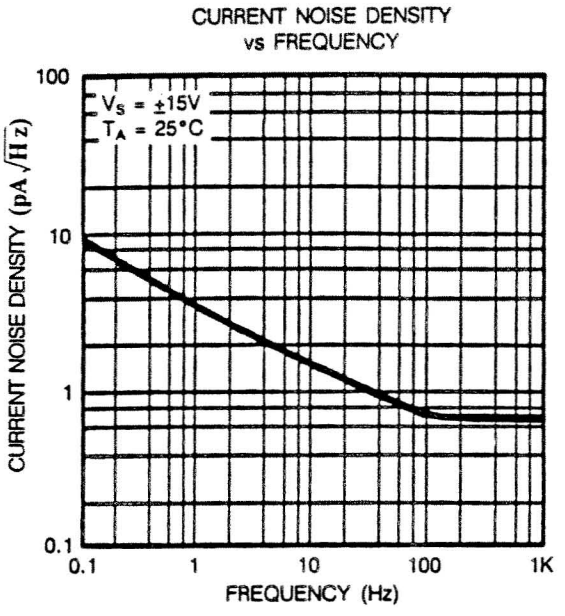


Figure 5.4.5-2.
Current Noise Density

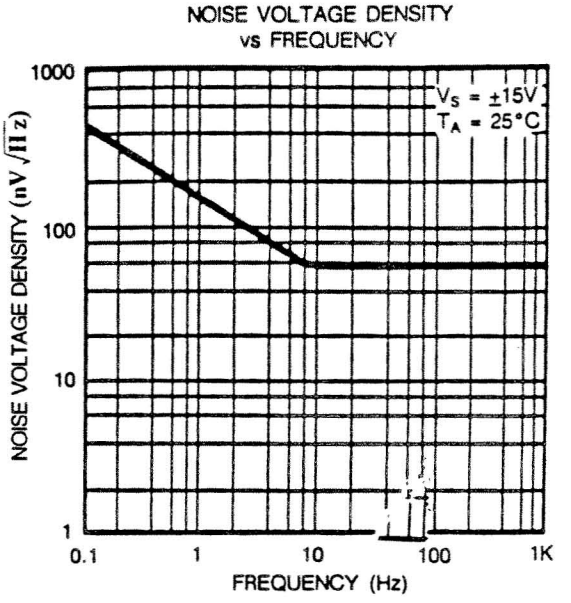


Figure 5.4.5-3.
Noise Voltage Density

Thus, based on Equation 5.4.5-1, the two thermal noise sources are equal to

$$V_{t1} = \{(4)(1.38E\text{-}23)(300)(900)(100\text{-}0.1)\}^{1/2} \qquad \text{(Eq. 5.4.5-5)}$$

or

$$V_{t1} = 0.038uv$$

and

$$V_{t2} = \{(4)(1.38E\text{-}23)(300)(10E3)(100\text{-}0.1)\}^{1/2} \qquad \text{(Eq. 5.4.5-6)}$$

or

$$V_{t2} = 0.129uv \ .$$

Next, the noise due to shot and contact are determined based on a combination of Equations 5.4.5-2 and 5.4.5-3.

$$I = in\{(f_{c1})\ln(f_h/f_1) + (f_h - f_1)\}^{1/2} \qquad \text{(Eq. 5.4.5-7)}$$

where "fc1" is the corner frequency (100 Hz) shown in Figure 5.4.5-2 and "in" is the current at 1 kHz (at least one decade above the corner).

Thus,

$$in = 0.7p(Hz)^{1/2} \qquad \text{(Eq. 5.4.5-8)}$$

is the current noise and would result in the current of

$$I = 0.7p\ \{(100)\ln(100/0.1) + (100 - 0.1)\}^{1/2} \qquad \text{(Eq. 5.4.5-9)}$$

or

$$I = 19.68\ \text{pArms}.$$

Therefore, the voltage noise would be

$$V_1 = (19.68\text{pArms})(900) = 0.017\text{uvrms} \qquad \text{(Eq. 5.4.5-10)}$$

and

$$V_2 = (19.68\text{pArms})(10\text{K}) = 0.197\text{uvrms}. \qquad \text{(Eq. 5.4.5-11)}$$

Finally, the last noise voltage would be

$$V_3 = en\{(f_{ce})\ln(f_H/f_L) + (f_H - f_L)\}^{1/2} \qquad \text{(Eq. 5.4.5-12)}$$

where "f_{ce}" is the corner frequency (8 Hz) shown in Figure 5.3.5-3 and "en" is the noise voltage at 1 kHz (at least one decade above the corner). Thus,

$$en = 60nv/(Hz)^{1/2} \qquad \text{(Eq. 5.4.5-13)}$$

is the noise voltage and would result in the voltage (V_3) of

$$V_3 = 60\ nv\ \{(8)\ln(100/0.1) + (100 - 0.1)\}^{1/2} \qquad \text{(Eq. 5.4.5-1)}$$

$$V_3 = 0.747\text{uvrms}.$$

Therefore, the total RMS noise voltage becomes

$$V_T = \{Vt_1^2 + Vt_2^2 + V_1^2 + V_2^2 + V_3^2\}^{1/2} \qquad \text{(Eq. 5.4.5-15)}$$

or

$$V_T = 0.784\text{uvrms}$$

which corresponds to

$$V_T(3\ \sigma) = 2.352\ \text{uvrms}. \qquad \text{(Eq. 5.4.5-16)}$$

Therefore, the total noise referenced to the input would be equal to the total rms noise voltage times the closed loop gain.

5.4.6 AC Sensitivity

AC sensitivity analysis is one of the least understood design tools but one of the most important. Typically, sensitivity does not tell you the percentage change in a parameter due to a component change, nor will it tell you how tolerance or the correlation between component values affect a particular parameter. Instead, sensitivity analysis tell of the relative "goodness" of the circuit by describing how the variations in one component affect a certain

performance of other components. This sensitivity analysis is sometimes referred to as Bode sensitivity. As an example of a sensitivity analysis, the following example will be used. It should be noted that in circuit simulation, ac sensitivity is usually performed at a frequency of interest. For example, if a circuit has a resonant peak at 1 kHz, the ac sensitivity analysis should occur at 1 kHz not at dc. AC sensitivity usually implies that a circuit is evaluated at a frequency.

$A = 3.50136$
$R_1 = R_2 = 1$
$C_1 = C_2 = 0.47148$
$W_o = 1$

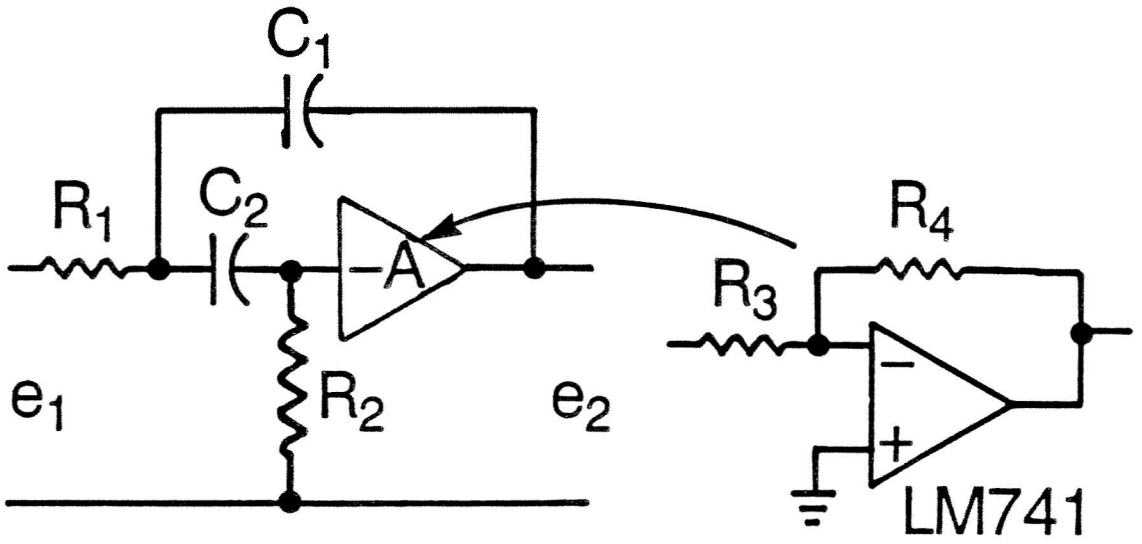


Figure 5.4.6.1. Sallen - Key Circuit

As an example, the ac sensitivity (Q only) of a Sallen Key filter shown in Figure 5.4.6-1 will be determined. First, the transfer function is derived as

(Eq. 5.4.6-1)

$$\frac{e_2}{e_1} = \frac{-\left[\frac{A}{(A+1)\,R_1C_1}\right] s}{s^2 + \left[\frac{R_1C_1 + R_2C_2 + R_1C_2}{(A+1)R_1R_2C_1C_2}\right] s + \frac{1}{(A+1)R_1R_2C_1C_2}}$$

with

$$Wo = \frac{1}{\{(A + 1)R_1R_2C_1C_2\}^{1/2}} \qquad \text{(Eq. 5.4.6-2)}$$

and

$$Q = \frac{\{(A + 1)R_1R_2C_1C_2\}^{1/2}}{\{R_1C_1 + R_2C_2 + R_1C_2\}^{1/2}} . \qquad \text{(Eq. 5.4.6-3)}$$

Next, determine the sensitivity of "Q" with respect to the gain "A" and component values. This is accomplished by taking the partial derivative of equation 5.4.6-3 with respect to A, R_1, R_2, C_1 and C_2 individually relative to "Q". Thus, the sensitivities are

$$S^Q_A = \frac{A}{2(A + 1)} = 0.39, \qquad \text{(Eq. 5.4.6-4)}$$

$$S^Q_{R1} = \frac{1}{2} - \frac{R_1C_1 + R_1C_2}{R_1C_1 + R_2C_2 + R_1C_2} = -0.167, \qquad \text{(Eq. 5.4.6-5)}$$

$$S^Q_{R1} = \frac{1}{2} - \frac{R_2C_2}{R_1C_1 + R_2C_2 + R_1C_2} = 0.167, \qquad \text{(Eq. 5.4.6-6)}$$

$$S^Q_{C1} = \frac{1}{2} - \frac{R_1C_1}{R_1C_1 + R_2C_2 + R_1C_2} = 0.167 \qquad \text{(Eq. 5.4.6-7)}$$

and

$$S^Q_{C2} = \frac{1}{2} - \frac{R_1C_2 + R_2C_2}{R_1C_1 + R_2C_2 + R_1C_2} = -0.167. \qquad \text{(Eq. 5.4.6-8)}$$

Another example with a simpler partial derivative is the Delyiannis - Friend filter.

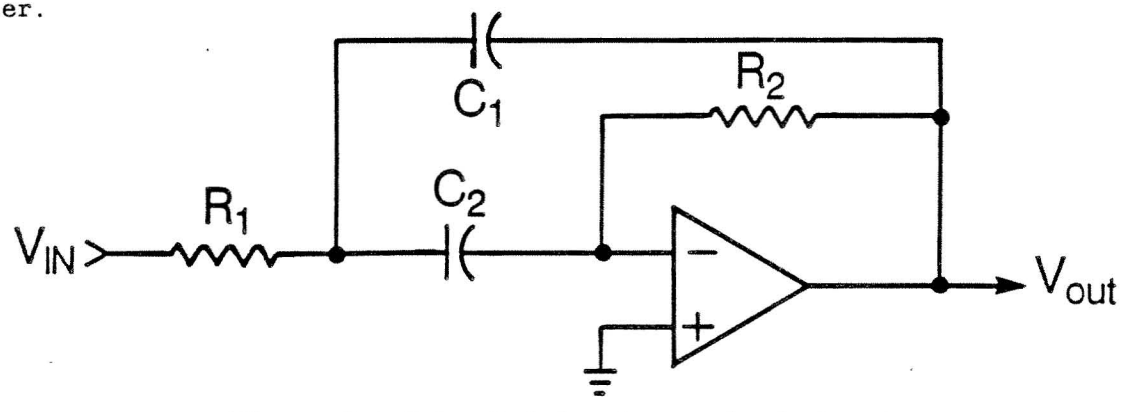


Figure 5.4.6-2. Delyiannis - Friend Circuit

The transfer function of the Delyiannis-Friend filter shown in figure 5.4.6-2 is

$$\frac{V_{out}}{V_{in}} = \frac{(-1/R_1C_1)s}{s^2 + (1/R_2)(1/C_1 + 1/C_2)s + 1/R_1R_2C_1C_2} \quad \text{(Eq. 5.4.6-9)}$$

If C_1 and C_2 are equal, then the transfer function reduces to

$$\frac{V_{out}}{V_{in}} = \frac{(-1/R_1C)s}{s^2 + (2/R_2C)s + 1/R_1R_2C^2} \quad \text{(Eq. 5.4.6-10)}$$

where

$$w_o = 1/C\ (R_1R_2)^{1/2} \quad \text{(Eq. 5.4.6-11)}$$

and

$$Q = (1/2)\{R_1/R_2\}^{1/2} \quad . \quad \text{(Eq. 5.4.6-12)}$$

The sensitivity of "Q" with respect to the resistors is determined by taking the partial derivative at equation 5.4.6-12 with respects to "Q" to R_1 and R_2. Thus,

$$S^{Q}_{R1} = -1/4 \quad \text{(Eq. 5.4.6-13)}$$

and

$$S^{Q}_{R2} = +1/4 \quad \text{(Eq. 5.4.6-14)}$$

The sensitivity of w_o to the passive components is

$$S^{wo}_{C} = -1, \quad \text{(Eq. 5.4.6-15)}$$

and

$$S^{wo}_{R1} = -1/2 \quad \text{(Eq. 5.4.6-16)}$$

and

$$S^{wo}_{R2} = -1/2 \quad \text{(Eq. 5.4.6-17)}$$

Once the sensitivities are determined, it will be possible to show how component variations change sensitivities.

5.4.7 Other Analysis Tools (Transfer Function Derivation)

A unique method of deriving transfer functions is using Nathan's method for admittance matrix reduction. Then use the conventional Cramer's rule

for solving for the transfer function. For example, support it is desired to derive the transfer function for Figure 5.4.7-1. Using conventional techniques, this could be very tricky but using Nathan's method a solution can be derived as follows. First, assign node number to every node except ground. Next, determine the short circuit admittance matrix. It should be noted that all admittance off of the major diagonal are expressed as negative admittances. Since V_3 is essential at zero volts everything that V_3 multiplies in the admittance matrix is equal to zero volts also. Therefore, column 3 in equation 5.4.7-1 can be eliminated. The current I_4 is the only dependent current variable and it is dependent upon V_3. Therefore, the I_4 current can be eliminated.

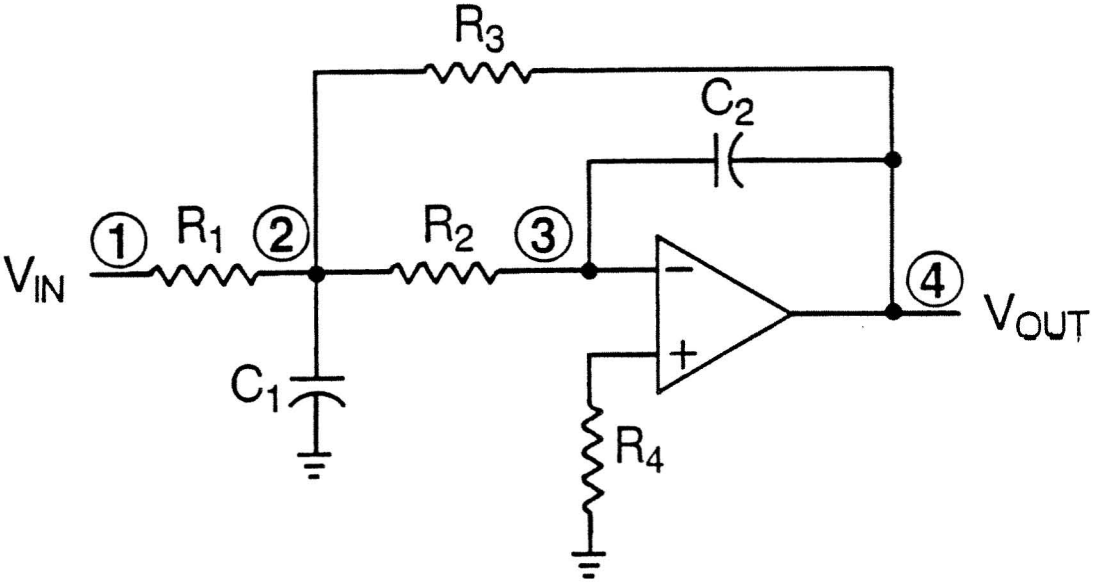


Figure 5.4.7-1. Example Circuit

Thus, the admittance matrix is reduced to

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ \cancel{I_4} \end{bmatrix} = \left[\begin{array}{cccc} 1/R_1 & -1/R_1 & 0 & 0 \\ -1/R_1 & Y_a & -1/R_2 & -1/R_3 \\ \cancel{0} & \cancel{-1/R_2} & \cancel{Y_b} & \cancel{-sC_2} \\ 0 & -1/R_3 & -sC_2 & Y_c \end{array}\right] \begin{bmatrix} V_1 \\ V_2 \\ \cancel{V_3} \\ V_4 \end{bmatrix} \quad \text{(Eq. 5.4.7-1)}$$

where

$$Y_{22} = Y_a = 1/R_1 + 1/R_2 + 1/R_3 + sC \quad \text{(Eq. 5.4.7-2)}$$

$$Y_{33} = Y_b = 1/R_2 + {}^{s}C_2 \quad \text{(Eq. 5.4.7-3)}$$

and

$$Y_{44} = Y_c = 1/R_3 + sC_2 \qquad \text{(Eq. 5.4.7-4)}$$

Cramer's rule states that desired voltage is solved by substituting the current vector into the admittance matrix column corresponding to the voltage of interest. Then, the results are divided by the determinate of the admittance matrix. When solving for the transfer function, this is not necessary. Instead, solve for Vont/Vin directly from the system matrix.

Therefore, the admittance matrix reduces to a ratio of two system matrixes for their associated admittance, $Y_1{}^4$ and $Y_1{}^1$ or

$$Y_1{}^4 = \begin{bmatrix} 1/R_1 & -1/R_1 & 0 \\ -1/R_1 & Y_a & -1/R_3 \\ 0 & -1/R_2 & -sC_2 \end{bmatrix} \qquad \text{(Eq. 5.4.7-5)}$$

and

$$Y_1{}^1 = \begin{bmatrix} 1/R_1 & -1/R_1 & 0 \\ -1/R_1 & Y_a & -1/R_3 \\ 0 & -1/R_2 & -sC_2 \end{bmatrix} \qquad \text{(Eq. 5.4.7-6)}$$

thus

$$\frac{V_{out}}{V_{in}} = \frac{Y^1{}_4}{Y^1{}_1} = \frac{\begin{matrix} -1/R_1 & Y_a \\ 0 & -1/R_2 \\ Y_a & -1/R_3 \\ -1/R_2 & sC_2 \end{matrix}}{} = \frac{1/R_1R_2}{YasC_2 - 1/R_2R_3} \qquad \text{(Eq. 5.4.7-7)}$$

or

$$\frac{V_{out}}{V_{in}} = \frac{-R_3/R_1}{s^2\, C_1C_2R_1R_2/R_3 + s\, C_2R_2/R_3\, (1/R_1 + 1/R_2 + 1/R_3) + 1} \qquad \text{(Eq. 5.4.7-8)}$$

becomes the transfer function for the example circuit.

NOTE: The determinant of a matrix of order greater than three is not trivial, so if your circuit has too many nodes, think of another approach for solving the transfer function.

5.5 TRANSIENT ANALYSIS

5.5.1 Impulse Response

The transfer function of a circuit can be determined by inputting an impulse and measuring the output voltage as a function of time. The transfer function, expressed in the frequency domain, is determined by taking the Laplace Transform of the output waveform.

5.5.2 Step Response

The step response of a circuit is a standard measure of the response of a circuit or system to a unit input step function. A step response, a function of time, can tell you whether your circuit is overdamped, critically damped or underdamped. The characteristic equation for a typical second order circuit is

$$s^2 + 2\xi\omega_n s + \omega_n^2 = 0, \qquad \text{(Eq. 5.5.2-1)}$$

Where "ξ" is the dampening ratio and "ω_n" is the natural frequency. The "ξ" of a circuit corresponds to the "Q", quality factor, in the relationship

$$Q = 1/2\ \xi. \qquad \text{(Eq. 5.5.2-2)}$$

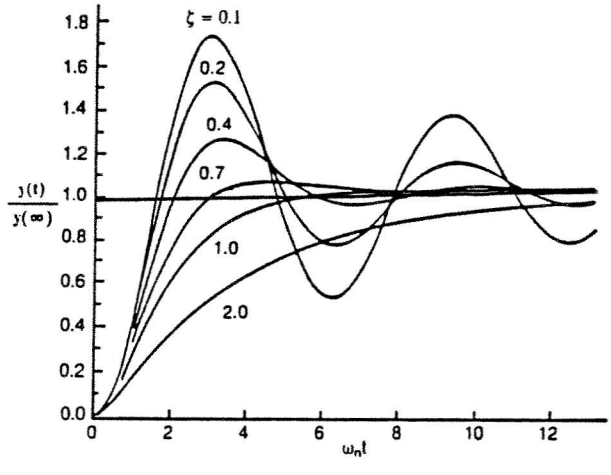


Figure 5.5.2-1. Step Response

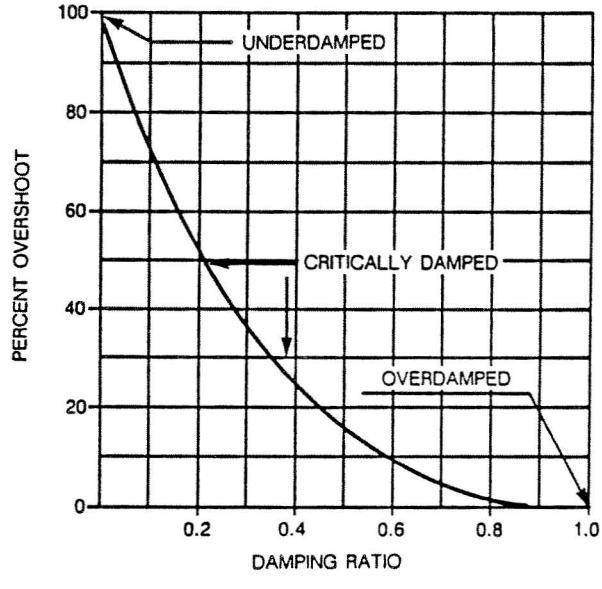


Figure 5.5.2-2. Overshoot vs "ξ"

As "ξ" gets smaller, "Q" gets larger and the amount of overshoot increases. In addition, as "ξ" gets smaller it takes less time for the circuit to intercept its final value as can be seen in Figure 5.4.2-1. The final value of a circuit can be determined by

$$\lim_{t \to \infty} h(t) = \lim_{s \to 0} sH(s) \qquad \text{(Eq. 5.5.2-3)}$$

or the Final Value Theorem. The H(s) in Equation 5.5.2-3 is the transfer function of the circuit times the Laplace transform of a unit step input (1/s).

Thus, Equation 5.5.2-3 could be rewritten for a step response (1/s) of a circuit G(s) as

$$\lim_{t\to\infty} h(t) = \lim_{s\to 0} s\left[\frac{G(s)}{s}\right] = G(o) \qquad \text{(Eq. 5.5.2-4)}$$

where

$$H(s) = \frac{G(s)}{s} \qquad \text{(Eq. 5.5.2-5)}$$

or the find value to a step response equals the transfer function evaluate at dc.

5.5.3 Initialization of a Circuit

It is occasionally necessary to determine the initial condition of a circuit or how the circuit will be initialized. Usually this requirement will be needed for a power-on reset which is used to reset digital logic. Sometimes the initialization will be needed due to multiple supply voltage which will need to be synchronized so as not to damage some components. Initialization of an analog circuit can be needed because of turn-on stability problems such as those seen in servo loops.

Other circuit requirements can include discharging energy storage devices at power-down or power line transient performance requirements.

Regardless of the requirement, the designer should attempt to get the broadest definition of what is required from this circuit.

5.5.4 Fourier Series

The Fourier series of a signal is a very important measurement that can be determined on a signal. Signal analysis is important because it can point to system or circuit performance issues. The Fourier series can be determined by the equation

$$c_n = \int_{-T/2}^{T/2} f(t)\ e^{-j\omega_n t}\ dt. \qquad \text{(Eq. 5.5.4-1)}$$

This, of course, requires f(t) to be a periodic waveform. A Fourier series can be constructed which can, based on the number of harmonies used, approximate the waveform being analyzed. The Fourier series may look something like

$$f(t) = c_0 + c_1 \cos(w_o t + \Phi_1) + \ldots + c_n \cos(nw_o t + \Phi_n) \qquad \text{(Eq. 5.5.4-2)}$$

Where "c_o" is the dc component of the waveform, "n" is the harmonic and "c_n" and "Φ_n" are the amplitudes and phases associated with the series. Usually, it is a good idea to use a computer program to get the Fourier Series. Once the series has been determined, the harmonic content can be analyzed to determine how the input waveform was distorted by the circuit. A measurement called total harmonic distortion, THD, can be determined by the equation

$$THD = \left(\frac{1}{c_1} \sum_{n=2}^{\infty} c_a \right) X\ 100 \qquad \text{Eq. 5.5.4-3)}$$

and is expressed in percent.

5.5.5 State Space Models

State space modeling of a transfer function is a convenient method of determining the transient or time dependent response of a circuit. As an example of this method, the following circuit will be considered.

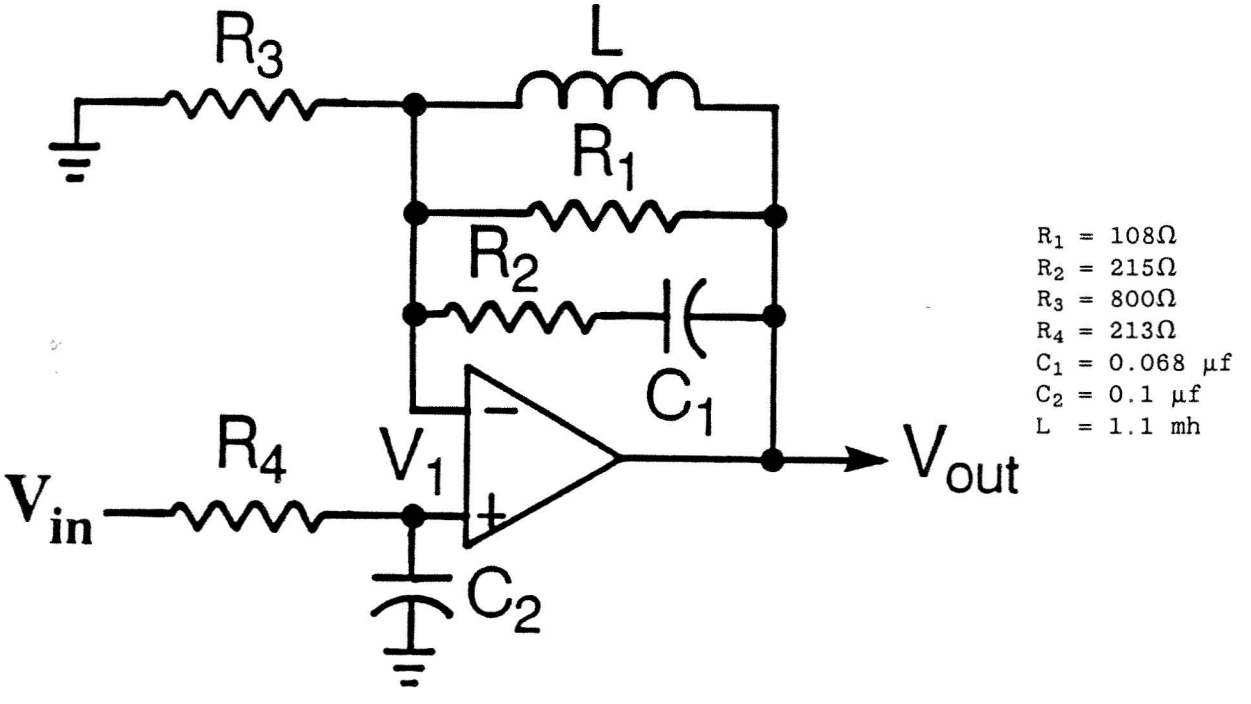


Figure 5.5.5-1.
Example Circuit

First, derive the transfer function for the example circuit shown in Figure 5.5.5-1. This can be done in two parts. The first part is

$$\frac{V_{out}}{V_1} = \frac{\dfrac{s^2\,(R_1R_2LC_1) + s\,(R_1L)}{s^2(R_2LC_1)+R_1LC_1)+s(R_1R_2C_1+L) + R_1 + 1}}{R_3} \qquad \text{(Eq. 5.5.5-1)}$$

or with variable substitution

$$\frac{V_{out}}{V_1} = \frac{\dfrac{As^2 + Bs}{cs^2 + Ds + E + 1}}{R_3} \qquad \text{(Eq. 5.5.5-2)}$$

or

$$\frac{V_{out}}{V_1} = \frac{1(A/R_3C)s^2 + (B/R_3C)s + 1}{s^2 + (D/C)s + (E/D)} \qquad \text{(Eq. 5.5.5-3)}$$

or

$$\frac{V_1}{V_1} = \frac{(A/R_3C + 1)s^2 + (B/R_3C + D)s + (E/C)}{s^2 + (D/C)s + (E/C)} \; . \qquad \text{(Eq. 5.5.5-4)}$$

Next, let

$$K_1 = A/R_3C + 1, \qquad \text{(Eq. 5.5.5-5)}$$

$$K_2 = B/R_3C + D, \qquad \text{(Eq. 5.5.5-6)}$$

$$K_3 = E/C \qquad \text{(Eq. 5.5.5-7)}$$

and

$$K_4 = D/C. \qquad \text{(Eq. 5.5.5-8)}$$

Thus, Equation 5.5.5-4 can be rewritten as

$$\frac{V_1}{V_1} = \frac{K_1s^2 + K_2s + K_3}{s^2 + K_4s + K_3} \; . \qquad \text{(Eq. 5.5.5-9)}$$

The second part of the transfer function becomes

$$\frac{V_{out}}{V_{in}} = \frac{1}{sR_4C_2 + 1} = \frac{1/R_4C_2}{s + 1/R_4C_2} \qquad \text{(Eq. 5.5.5-10)}$$

and let

$$K_5 = 1/R_4C_2. \qquad \text{(Eq. 5.5.5-11)}$$

Thus, Equation 5.5.5-10 becomes

$$\frac{V_1}{V_{in}} = \frac{K_5}{s + K_5} \qquad \text{(Eq. 5.5.5-12)}$$

Next, multiply through both Equations 5.5.5-9 and 5.5.5-12 by the inverse of the highest order of s. This will result in

$$\frac{V_{out}}{V_1} = \frac{K_1 + K_5 s^{-1} + K_3 s^{-2}}{1 + K_4 s^{-1} + K_3 s^{-2}} \qquad \text{(Eq. 5.5.5-13)}$$

and

$$\frac{V_1}{V_{in}} = \frac{K_5\ s^{-1}}{1 + K_5\ s^{-1}}\ . \qquad \text{(Eq. 5.5.5-14)}$$

The state space model for V_1/V_{in} will be developed first. All state space model will use the summation output as the reference point for determining the state space model. Thus, the output of the summation is equal to

$$e_1(s) = V_{in} - K_5\ e_1(s)s^{-1}. \qquad \text{(Eq. 5.5.5-16)}$$

Next, it is necessary to determine what the output voltage, V_1, would be equal to or

$$V_1 = K_5 s^{-1}\ e_1(s) \qquad \text{(Eq. 5.5.5-17)}$$

where

$$\frac{V_1}{V_{in}} = \left[\frac{e_1(s)}{V_{in}}\right]\left[\frac{V_1}{e_1(s)}\right]\ . \qquad \text{(Eq. 5.5.5-18)}$$

Combining Equations 5.5.5-16 and 5.5.5-17 into a figure produces Figure 5.5.5-2.

Next, the second part of the State Space Model is determined.

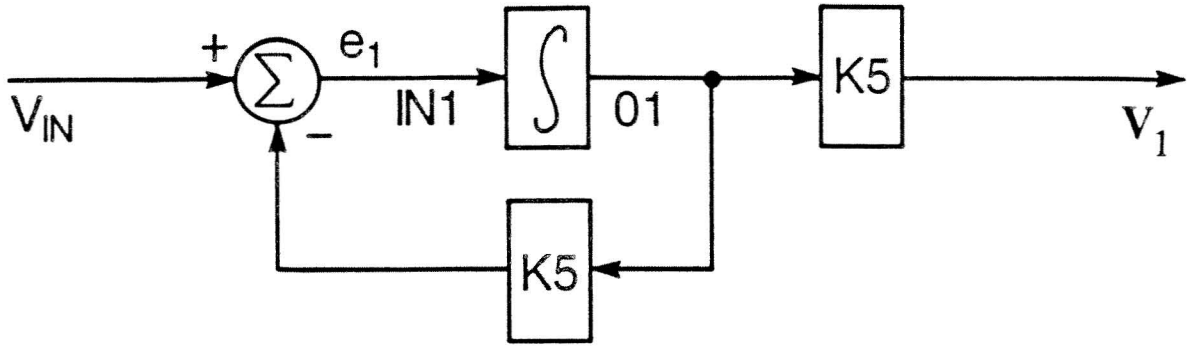


Figure 5.5.5-2. State Space Model (Part One)

The state space model for Vout/V_1 is developed based on the intermediate summation point output, $e_2(s)$. Thus, the output of the summation is equal to

$$e_2(s) = \frac{V_1}{1 + K_4 s^{-1} + K_3 s^{-2}} \qquad \text{(Eq. 5.5.5-19)}$$

or

$$e_2(s) = V_1 - e_2 K_4 s^{-1} - e_2 K_3 s^{-2} \qquad \text{(Eq. 5.5.5-20)}$$

Next, it is necessary to determine what the output voltage, V_{out}, would be equal to as

$$V_{out} = (K_1 + K_2 s^{-1} + K_3 s^{-2}) e_2(s) \qquad \text{(Eq. 5.5.5-21)}$$

where

$$\frac{V_{out}}{V_1} = \left[\frac{e_2(s)}{V_1}\right]\left[\frac{V_{out}}{e_2(s)}\right] \qquad \text{(Eq. 5.5.5-22)}$$

Combining Equations 5.5.5-20 and 5.5.5-21 into a figure produces Figure 5.5.5-3.

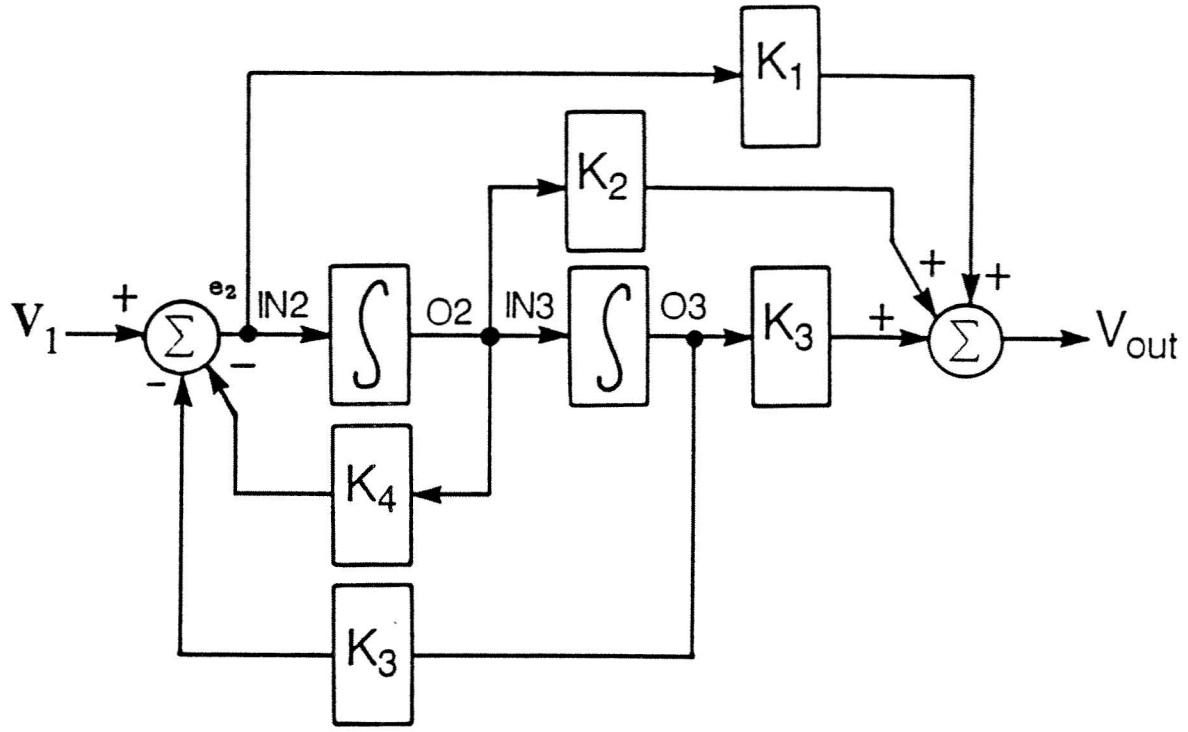


Figure 5.5.5-3. State Space Model (Part Two)

A computer program can now be directly written from the two block diagrams and using numerical integration techniques. Then the step response shown in Figure 5.5.5-4 (or any other transient response) can be determined.

```
LIST

100C/HOME/PRO
101 CALL ATTACH(10,"/HOME/DATA;",2,0,I1,)
110 REAL L,K1,K2,K3,K4,K5
112 REAL 01,02,03,IN1,IN3
120 DATA R1,R2,R3,R4/108.0,215.0,800.0,215.0/
121C All integrator ouputs zeroed
122 DATA 01,02,03/0.0,0.0,0.0/
124 DATA VIN,DT,T,H/1.0,0.000001,0.0,0.0/
140 A=R1*R2*L*C1
130 DATA C1,C2,L/0.068E-6,0.1E-6,1.1E-3/
140C Define variables
150 B=R1*L
160 C=(R2*L*C1)+(R1*L*C1)
170 D=R1*R2*C1+L
180 E=R1
190 K1=(A/(C*R3))+1.0
200 K2=(B/(C*R3))+(D/C)
210 K3=E/C
220 K4=D/C
230 K5=1/R4*C2
240 IF(T.LE.0.0) GOTO 20
245 30 CONTINUE
```

```
246C Describes block diagrams with respect to
247C input and important points
250 IN1=VIN-O1*K5
260 IN2=O1*K5-O2*K4-O3*K3
270 IN3=O2
280 VOUT=O3*K3+O2*K2+IN2*K1
285C Increment integration
290 O1=O1+DT*IN1
300 O2=O2+DT*IN2
310 O3=O3+DT*IN3
315C Increment time
320 T=T+DT
345 20 CONTINUE
350 WRITE(10,60)T, VIN, VOUT
355C Loop until 2 miliseconds worth calculated
360 IF(T.LT.0.002) GOTO 30
390 60 FORMAT(1X,3(1X,1PE10.3))
400 STOP;END
```

*Use Euler's numerical integration technique

5.6 OTHER ANALYSIS

5.6.1 Worst Case and 3 Sigma

For a Normal (Gaussian) Distribution 3σ is a good approximation of the worst case performance. A +/- 3σ distribution will include 99.75 percent of all possible samples. Based on the Central-Value theorem, the convolution of multiple non-Gaussian probability density functions will approach a net normal probability density function regardless of the shape of the individual probability density functions. In other words, a uniform density function of resistor R1 convolved with a Student-T distribution of resistor R2 convolved with a F distribution of resistor R3 will produce a net normal or Gaussian distribution for the resistors combined.

Usually, worst case analysis assumes that the worst case performance occurs at the minimal or maximum values of all components. This may or may not be the actual worst case because interactions between components is usually ignored in the worst case analysis. An example of this problem can be explained by use of the following example circuit shown in Figure 5.6.1-1.

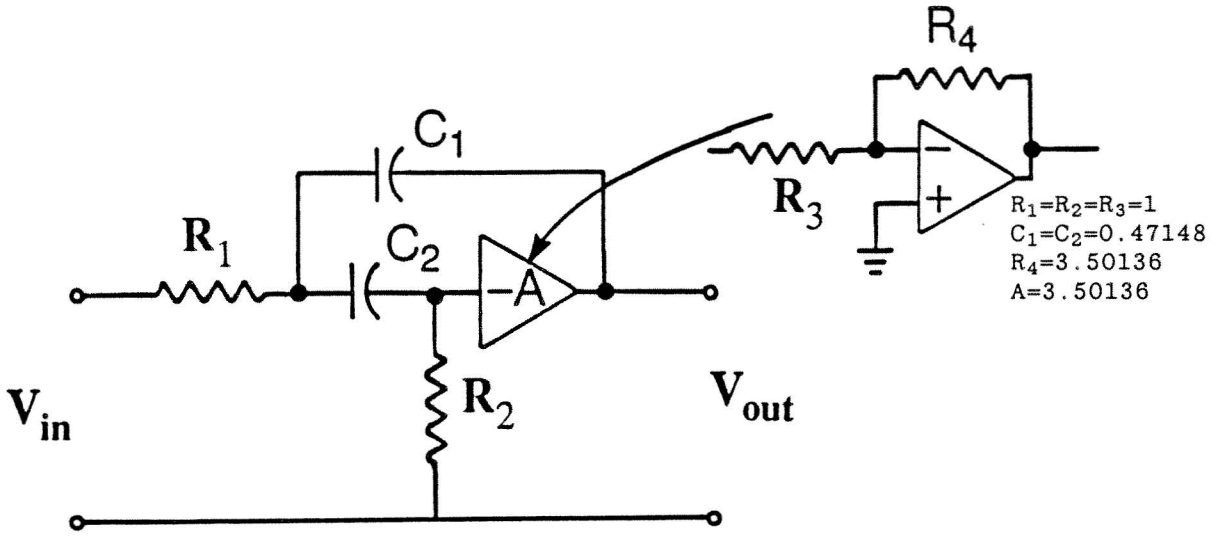


Figure 5.6.1-1. Sample Circuit

The transfer function for the circuit in Figure 5.6.1-1 is

$$\frac{V_{out}}{V_{in}} = \frac{-\left[\left(\frac{A}{A+1}\right) R_1C_1\right] s}{s^2 + \left(\frac{R_1C_1 + R_2C_2 + R_1C_2}{(A+1)\ R_1R_2C_1C_2}\right) s + \frac{1}{(A+1)\ R_1R_2C_1C_2}} \qquad \text{(Eq. 5.6.1-1)}$$

If R_1, R_2, C_1 and C_2 have a ±10 percent tolerance each and "A" is fixed, a computer simulation (see Tables 5.6.1-1 and 5.6.1-2) shows that "worst case" performance based on using maximum and minimum tolerance produces an ac frequency response variation of

$$V_{out} = 0.6404 \text{ volts } \pm 19 \text{ percent.} \qquad \text{(Eq. 5.6.1-2)}$$

Table 5.6.1-1.

RPS	Magnitude Actual	Decibel Actual	Angle Actual
1.000D 00	6.4039D-01	-3.8711	-157.2235

PI=-6.4039091D-01

********** AFTER THE CALCULATIONS **********

COMPONENT	OLD	NEW
R1	1.0000D 00	9.0000D-01
R2	1.0000D 00	1.1000D 00
C1	4.7148D-01	4.2433D-01
C2	4.7148D-01	5.1863D-01

RPS	Magnitude Actual	Decibel Actual	Angle Actual
1.000D 00	7.6237D-01	-2.3567	-154.7457

Table 5.6.1-2.

RPS	Magnitude Actual	Decibel Actual	Angle Actual
1.000D 00	6.4039D-01	-3.8711	-157.2235

PI=-6.4039091D-01

********** AFTER THE CALCULATIONS **********

COMPONENT	OLD	NEW
R1	1.0000D 00	1.1000D-01
R2	1.0000D 00	9.0000D 01
C1	4.7148D-01	5.1863D-01
C2	4.7148D-01	4.2433D-01

RPS	Magnitude Actual	Decibel Actual	Angle Actual
1.000D 00	5.2508D-01	-5.5954	-158.8628

Table 5.6.1-3

FOR NOMINAL VALUES OF THE PARAMETERS

RPS	OUTPUT	MAGNITUDE	DB	ANGLE
1.0000D 00	VOLTS	6.4039091D-01	-3.8711	-157.2235

HISTOGRAM FOR OUTPUT VOLTS AT FREQUENCY 1.0000000D 00 RPS
MAGNITUDE MEAN = 6.31735D-01 STANDARD DEVIATION = 6.22325D-02

```
4.14704D-01  I
           2  I
4.35373D-01  I
           1  I
4.56042D-01  I
           4  I:
4.76711D-01  I
           6  I:
4.97380D-01  I
          21  I:::::
5.18049D-01  I
          26  I::::::
5.38718D-01  I
          60  I:::::::::::::::
5.59387D-01  I
          82  I::::::::::::::::::::
5.80056D-01  I
         103  I:::::::::::::::::::::::::::
6.00725D-01  I
         130  I::::::::::::::::::::::::::::::::
6.21394D-01  I
         141  I::::::::::::::::::::::::::::::::::::
6.42063D-01  I
         121  I::::::::::::::::::::::::::::::
6.62732D-01  I
         109  I:::::::::::::::::::::::::::
6.83401D-01  I
          76  I::::::::::::::::::
7.04070D-01  I
          42  I::::::::::
7.24739D-01  I
          37  I:::::::::
7.45408D-01  I
          23  I::::::
7.66077D-01  I
           8  I::
7.86746D-01  I
           5  I:
8.07415D-01  I
           3  I:
8.28084D-01  I
```

However, if a Monte Carlo analysis (see Table 5.6.1-3) were performed on the same circuit, the 3σ spread would be closer to ±30 percent using randomly selected valued for R_1, R_2, C_1, and C_2 within the ±10 percent tolerance window. Therefore, it can be concluded that worst case analysis in implementation may not give the worst case performance.

5.6.2 Monte Carlo and Histograms

Monte Carlo analysis is a term used for calculating a series of responses on a circuit where before each response is determining all components which have been so specified to have a tolerance associated with them are randomly changed to be equal to some value within their respective tolerance range.

As a result of multiple runs, a histogram or graphical representation of all of the responses can be constructed and used to determine the distribution of the output responses. As was shown in paragraph 5.6.1, Monte Carlo analysis would be preferred over worst case analysis if the worst case analysis does not consider the interaction between components.

5.6.3 Temperature Coefficients

One of the typical variables which affects the performance of virtually every circuit is temperature. In the military electronics arena, the military temperature range are the temperatures of concern. The military temperature range is -55°C to +70°C. From a components standpoint, almost every component value will changes as temperature changes. The change could be either an increase or decrease in value. Components which increase in value with an increase in temperature are said to have a positive temperature coefficient. Components which decrease in value with an increase in temperature are said to have a negative temperature coefficient. Usually, the temperature coefficient is expressed in terms of ± x ppm (parts per million)/°C or the temperature coefficient may be expressed as ±5 percent at -50°C and ±10 percent at 70°C. Temperature coefficient is a measure of the change due to temperature of a component.

Semiconductor devices are also affected by temperature. One example of a part which can be selected relative to its low temperature coefficient is a zener diode. A 5.0 volt zero diode will have a temperature coefficient of from 0 to +2 mv/°C over the temperature range from -55°C to +150°C. From a 21°C nominal temperature at 5.0 volt, zener diodes would have a value of

$$V_z \Big|_{T = 150°C} = 5.26 \text{ Vdc} \qquad \text{(Eq. 5.6.3-1)}$$

or

$$V_z \Big|_{\text{thus } T = -55°C} = 4.84 \text{ Vdc} \qquad \text{(Eq. 5.6.3-2)}$$

$$V_z = 5.0 \text{ Vdc } \pm 5 \text{ percent} \qquad \text{(Eq. 5.6.3-3)}$$

over temperature worst case.

Temperature compensated diodes can do the same thing a zener diode selected at 5.0 volts; however, the temperature compensated diodes will typically require more current.

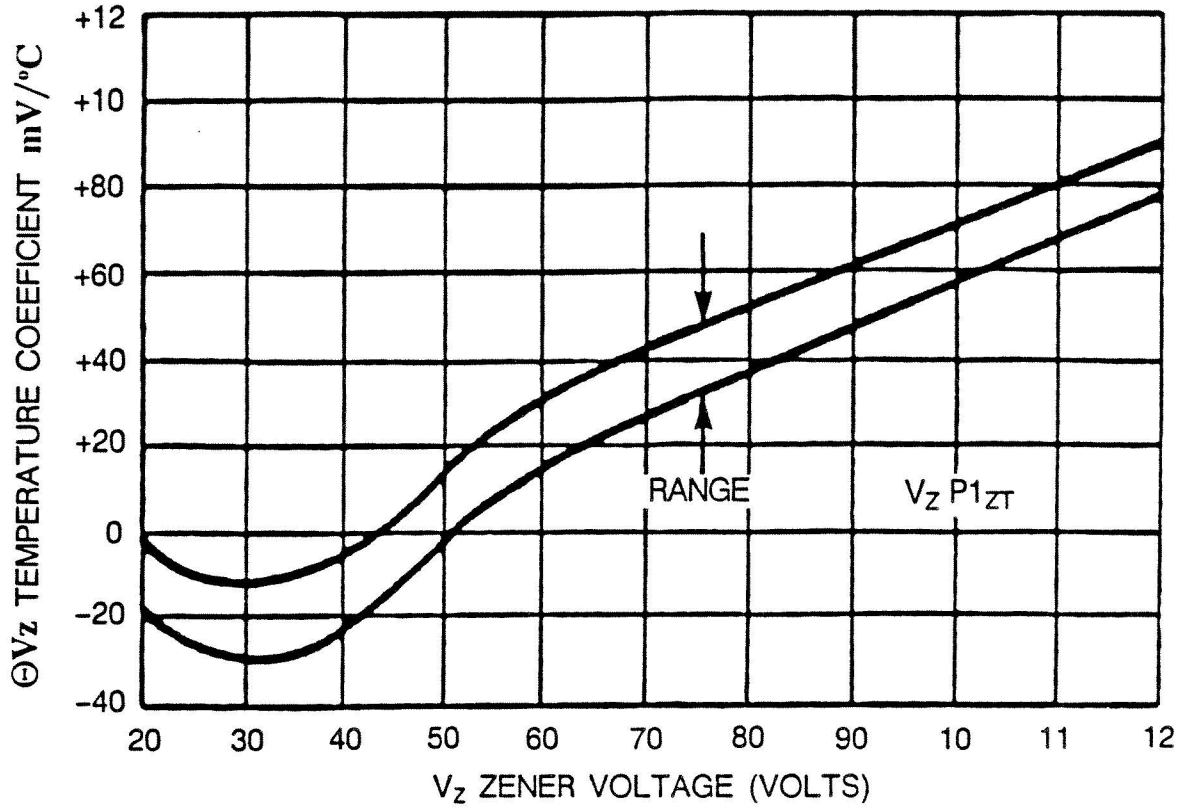


Figure 5.6.3-1. Effects of Temperature

Semiconductor devices are affected by temperature in other ways too. Thermal runaway is a condition where in a transistor I_{cbo} is temperature dependent. Suppose the I_c of a transistor causes the junction temperature to rise. As temperature rises, I_{cbo} increases which increases I_c. With I_c increasing, the junction temperature continues to rise which increases I_{cbo}. This process can continue until either the transistor burns out or is changed from operation in its active region to operating in its saturation region.

5.6.4 Error Budget Analysis

Error analysis or error budget analysis is usually required to show that a circuit or system meets the performance requirements. For example, suppose the performance requirement for an output voltage is ±5 percent. The circuit or system contains ten error sources of

$$e_1=e_2=e_3=e_4 = \pm 1 \text{ percent (worst case)}, \qquad \text{(Eq. 5.6.4-1)}$$

$$e_5=e_6=e_7=e_8 = \pm 2 \text{ percent (worst case)}, \quad \text{(Eq. 5.6.4-2)}$$

$$e_9 = \pm 5 \text{ percent (worst case)} \quad \text{(Eq. 5.6.4-3)}$$

and

$$e_{10} = \pm 10 \text{ percent (worst case)}. \quad \text{(Eq. 5.6.4-4)}$$

The worst case performance would be the sum of all the worst case errors or ±23%. in this case. This is well outside the performance requirement. Suppose all the errors are converted to their ±1σ errors and a worst case error performance is derived from the ±1σ errors or

$$e_1=e_2=e_3=e_4 = \pm 0.33 \text{ percent } (1\sigma), \quad \text{(Eq. 5.6.4-5)}$$

$$e_5=e_6=e_7=e_8 = \pm 0.67 \text{ percent } (1\sigma), \quad \text{(Eq. 5.6.4-6)}$$

$$e_9 = \pm 1.67 \text{ percent } (1\sigma) \quad \text{(Eq. 5.6.4-7)}$$

and

$$e_{10} = \pm 3.3 \text{ percent } (1\sigma) \quad \text{(Eq. 5.6.4-8)}$$

and

$$e_T = e_1 + e_2 + e_3 + e_4 + e_5 + e_6 + e_7 + e_8 + e_9 + e_{10}. \quad \text{(Eq. 5.6.4-9)}$$

The total errors can now be combined to show whether the circuit will meet the performance requirement. The error sources can be summed together to give a ±1σ worst case of ±8.96% (±1σ). However, this is not the suggested approach. Instead, use the RSS of the ±1σ errors as the gauge to measure the performance requirements or

$$e_T = \{e_1^2+e_2^2+e_3^2+e_4^2+e_5^2+e_6^2+e_7^2+e_8^2+e_9^2+e_{10}^2\}^{1/2} \quad \text{(Eq. 5.6.4-10)}$$

or

$$e_T = \{4(0.33)^2 + 4(.067)^2 + (1.67)^2 + (3.33)^2\}^{1/2} \quad \text{(Eq. 5.6.4-11)}$$

or

$$e_T = \pm 4 \text{ \% RSS } (1\sigma). \quad \text{(Eq. 5.6.4-12)}$$

Since the original performance requirement was not fully defined, the circuit designer needs only to add the RSS ±1σ qualifier onto the performance requirements to ensure that the circuit will pass. Otherwise, the tolerances must be adjusted to meet the worst case or ±1σ worst case performance requirements.

5.6.5 Cost Analysis

Cost analysis is an important determination that the engineer must make throughout the design process. Many times it is the cost of something that kills a design and not its electrical performance. Therefore, the designer should spend some time becoming familiar with how a cost analysis on a design can be performed.

Component cost on your circuit can vary dramatically based on whether you specify commercial, industrial, or military grade components. Typically, commercial components are the cheapest but they are the least reliable. Military grade components can be very expensive and very reliable. Generally, the operating temperature range of the system will help you define which type of part you can use. The military component temperature range is wider than the industrial or commercial.

Component selection may be further restricted based upon an approved parts list. This list of approved parts consists of all parts which can be used without the generation of a new source control drawing (SCD) for that part. Component Engineering can provide a list of approved parts for your program. However, it may be necessary to use a part which has no SCD yet. (IR&D or experimental circuits can use non-standard parts.)

Once a design is conceived and a component list (PL) is generated, the circuit designer can seek inputs from Reliability Engineering and Purchasing regarding the component that he has selected. It is feasible to acquire component cost from an outside distributer but official component cost must come from Purchasing. Reliability outputs directly affects the component cost because MTBF (mean time between failures) reflects in your expected circuit performance. If the MTBF is too low, higher reliability parts that cost more will need to be used.

An additional cost above and beyond the component cost is how much it will cost to manufacture. This manufacturing cost includes assembly, inspection, and support costs and depends upon the number of parts used and complexity of the design.

With the reliability, component cost and manufacturing cost information compiled, the circuit designer needs to supply this information to logistics along with any schematics, parts list, power requirements, etc., that are required. Logistics will then determine the total system's cost implication relative to your design. Usually, this cost analysis will balance the expected savings against the expected cost to determine whether the design should proceed.

5.7 DO I NEED . . .

5.7.1 Heat Sink

The question asked sometimes in a circuit design which contains large power dissipating devices is "Do I need a heat sink?" To answer this question, consider the following example. A five-volt regulator (LM309 type) has an input voltage of 9 volts dc and must source 0.5 amps for a power dissipation, P, of 2 watts. Is a heat sink required if the voltage regulator is required to operate a 75°C ambient? What would be the junction temperature for the device?

From Figures 5.7.1-1 to 5.7.1-4, it can be seen that only the LM109K in a TO3 case would be capable of operating without a heat sink. The LM109H in a TO3 case would require a 10°C/W heat sink. The LM309K in a TO3 case would require a 20°C/W heat sink. The LM309H in a TO3 case would require an infinite heat sink. Based on the device and case type, the requirement for a heat sink goes from no heat sink needed to an infinite heat sink required.

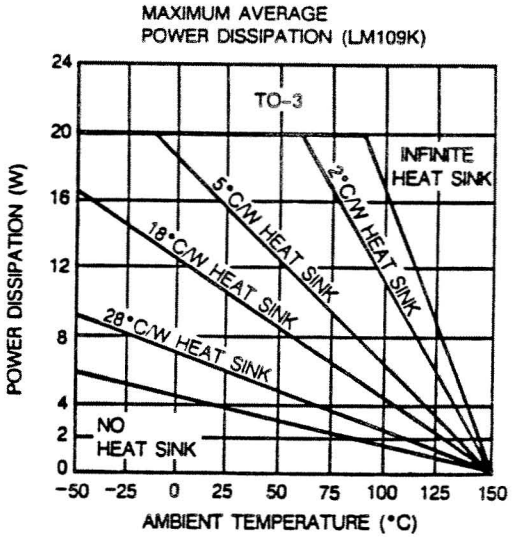


Figure 5.7.1-1

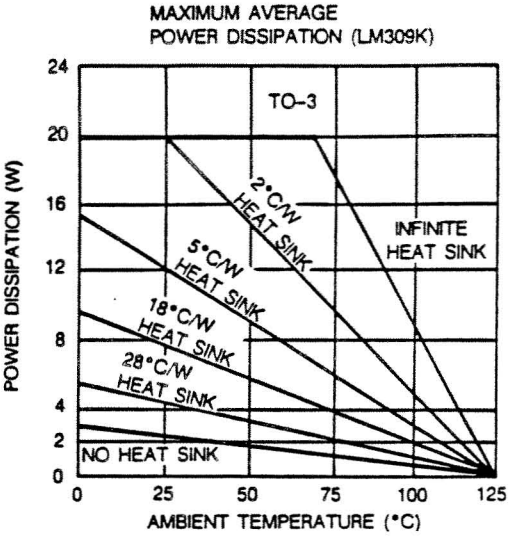


Figure 5.7.1-2

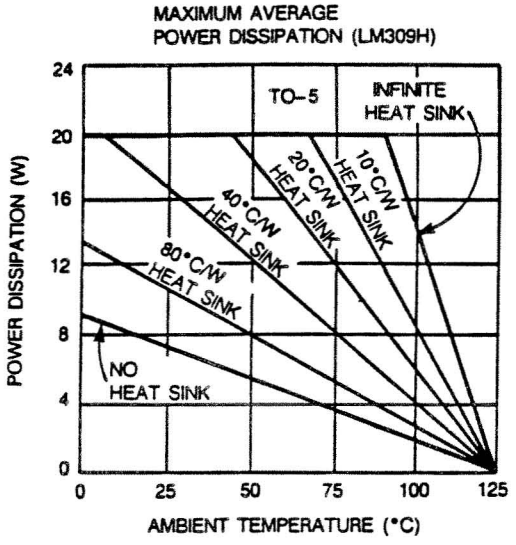


Figure 5.7.1-3.

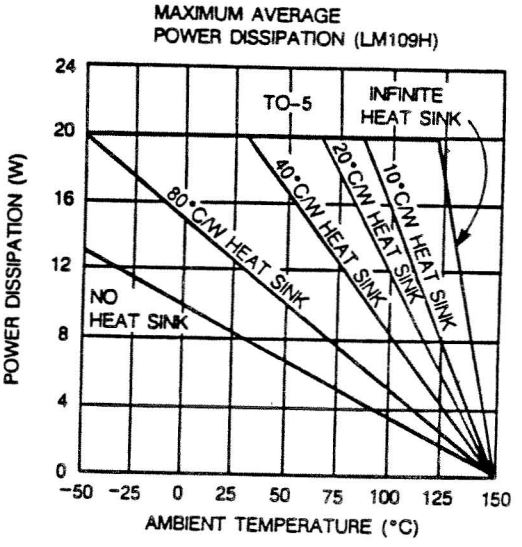


Figure 5.7.1-4

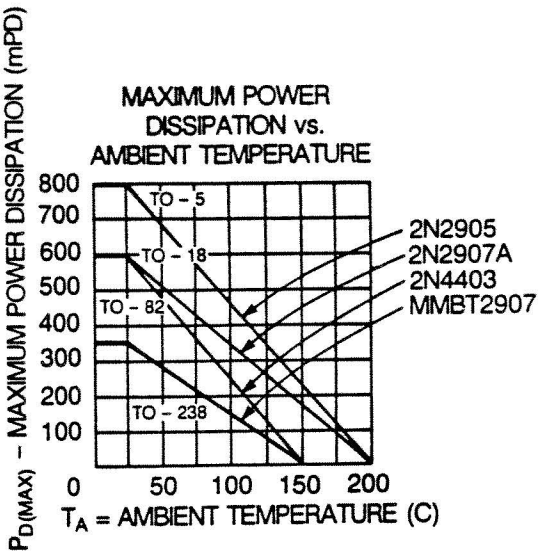


Figure 5.7.1-5.

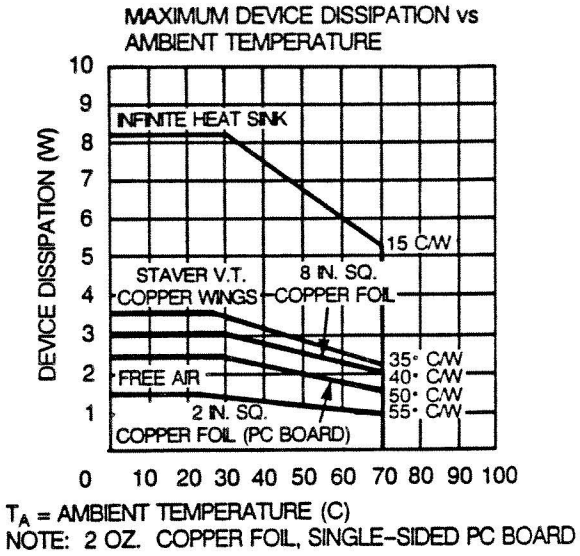


Figure 5.7.1-6

For other types of circuits, the questions of heat sinks may be partially answered by device (case) selection (see Figure 5.7.2-5) or the vendor may express a specific way to heat sink the device based on power dissipation and ambient temperature (see Figure 5.7.2-6). Based on the previous example, a 20°C/W heat sink would be required for a LM309K to be used.

One very important device parameter to consider is the junction temperature, T_J. Suppose that it is desired to keep the junction temperature below 50°C above ambient, T_A. Determine the required heat sink, R_{sa}.

For this example, it will be assumed that the junction to case thermal resistance, R_{jc}, is equal to 5°C/W and the case to heat sink, thermal resistance, R_{cs}, is equal to 0.5°C/W. The resulting equation for heat flow which would be analogous to Kirchoff's law would be

$$TJ - TA = PD\ (R_{sa} + R_{cs} + R_{jc}) \qquad \text{(Eq. 5.7.1-1)}$$

or

$$50^{0}C = 2\ \text{watts}\ (R_{sa} + 0.5^{0}C/W + 5.0^{0}C/W) \qquad \text{(Eq. 5.7.1-2)}$$

and

$$R_{sa} = 19.5^{0}sa = 19.5^{0}C/W. \qquad \text{(Eq. 5.7.1-3)}$$

Thus, a 20°C/W heat sink would be adequate to keep the junction temperature below 50°C above ambient.

5.7.2 Power Supply Decoupling

Power supply decoupling is a necessary fact of life. Few systems perform well without decoupling. Decoupling is needed because the power line is a common path for both internal and external noise sources. Usually, op-amps, voltage regulators, etc., have a certain amount of power supply rejection ratio

but this may not be enough isolation from noise. This is especially true at high frequencies because the power supply rejection ratio decreases as a function of frequency.

Typically, a low frequency capacitor is placed at the input of the supply voltage to the module. TEMPEST and EMI requirements typically drive the selection of these capacitors (and inductions if required). Usually, the low frequency capacitor will be a value from 2.2uf to 220uf based upon the performance requirements.

In addition to the low frequency capacitors, there is a need for high frequency capacitors also. These capacitors are typically (almost always) located directly across the IC's or transistor's power and ground pins. EMI performance requirements can drive the selection of the high frequency capacitors. Usually, the high frequency capacitor will be a value between 0.1uf to 0.001uf.

Many times, IC vendors will suggest the values for the decoupling capacitors. The designer should understand that there are system level performance issues that should be addressed before the selection is made. These would include power supply capacitive loading, switch noise (current surges), capacitor characteristics based on type (e.g. mylar, mica, polystyrene, etc.) and other performance goals.

5.7.3 Ground/Power Plane(s)

Typically, a ground plane is suggested for a printed circuit board for analog designs. Low level circuits which would be sensitive to ground currents should have a separate parallel ground connection altogether. Ground planes provide a low impedance path to the module's return. Power planes should also be considered because they provide a low impedance path back to the module's power input pin. In addition, at high frequencies, the power and ground planes act like another decoupling capacitor and balance the high frequency noise between the two planes.

5.8 THE PROBLEM WITH . . .

5.8.1 The Problem With Large Resistors

Large value resistors have two fundamental problems associated with them. First, the larger the resistor, the larger the thermal noise associated with that resistor. A relative order of magnitude may explain this. The relationship between thermal noise voltage, V_t, and resistance, R, is

$$V_t = \{4KTBR\}^{1/2} \qquad \text{(Eq. 5.8.1-1)}$$

where 4KTB equals the product between the Boltzmann's constant (1.38E-23 Joules/K), Absolute temperature (K) and noise bandwidth (B hertz). If the absolute temperature was 290 K, the noise bandwidth was 1 MHz and the resistance equal to 1 Kohms. Then the thermal noise would be equal to

$$V_t = \{(4)(1.38E\text{-}23)(290^0)(1E6)(1E3)\}^{1/2} \qquad \text{(Eq. 5.8.1-2)}$$

or

$$V_t = 4 \text{ uvolts.} \qquad \text{(Eq. 5.8.1-3)}$$

However, if the resistance were increased to 1 Mohm then the thermal noise

voltage would be equal to

$$V_t = \{(4)(1.38E\text{-}23)(290^0)(1E6)(1E6)\}^{1/2} \quad \text{(Eq. 5.8.1-4)}$$

or

$$V_t = 126.5 \text{ uvolts.} \quad \text{(Eq. 5.8.1-5)}$$

Thus, as the resistance goes up so does the thermal noise voltage.

Another important problem with large resistors is the shunt capacitance effect. If a 0.28pf shunt capacitance is assumed for a 1 Mohm resistor, then the real portion of the resistor's impedance at 500 kHz would be equal to

$$Re(j\omega) \Big|_{f=500 \text{ kHz}} = R/((\omega RC_2)^2+1) \quad \text{(Eq. 5.8.1-6)}$$

or

$$Re(j\omega) = 1E6/\{[(2\pi*1E6*0.28E\text{-}12)^2]+1\} = 563.7 \text{ Kohms.} \quad \text{(Eq. 5.8.1-7)}$$

Likewise, if a similar lower value resistor of 1 Kohm had the same 0.28 shunt capacitance, then the real portion of the resistor's impedance at 500 kHz would be equal to

$$Re(j\omega) = 1E3/\{[(2\pi*1E3*0.28E\text{-}12)^2]+1\} = 999.9 \text{ ohms.} \quad \text{(Eq. 5.8.1-8)}$$

Therefore, the larger the resistor, the larger the impact of the shunt capacitance.

There are two other minor points relative to large value resistors. First, not all resistors are created equal. A wire wound resistor has the smallest amount of generated noise voltage. Film type resistors have more noise voltage due to contact noise. Composition resistors have the greatest amount of noise because the material is nonhomogenous. Another factor to consider is that resistor of larger power ratings will have lower noise voltages compared to smaller power rated resistors of the same type.

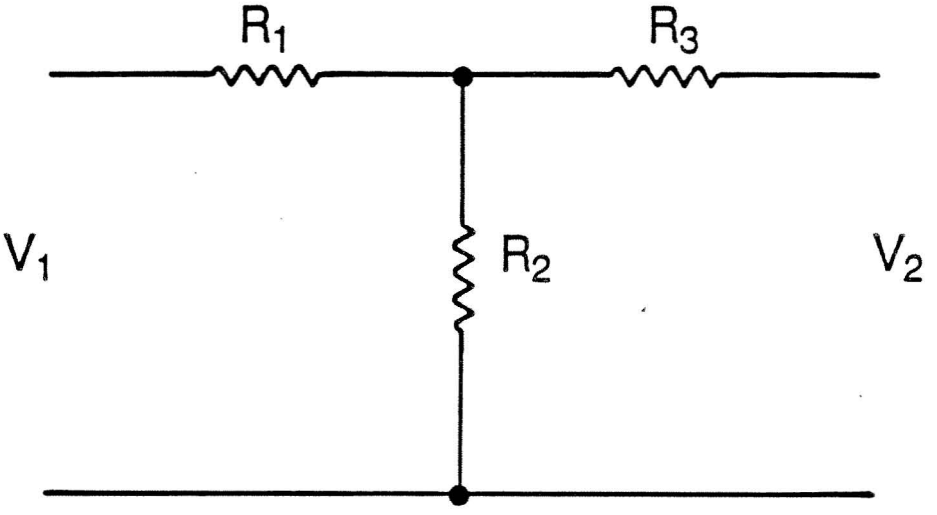


Figure 5.8.1-1. T-Network

One additional point to be made is equivalent resistance. A T-network can be used to obtain a short-circuit transfer impedance which is larger than any of the individual components used. Usually, the T-network will be used in the feedback of an op-amp circuit but it is not restricted to that application. The short-circuit transfer function for the T-network shown in Figure 5.8.1-1 is

$$Zsc = \frac{R_1R_2 + R_2R_3 + R_3R_1}{R_2} = \frac{V_1}{I_2}\Big|_{+ V_2 = 0} \qquad \text{(Eq. 5.8.1-9)}$$

If a Z_{sc} = 1 Mohm resistance is desired and

$$R_1 = R_3 = 10 \text{ Kohms} \qquad \text{(Eq. 5.8.1-10)}$$

then the value of R_2 will be

$$R_2 = \frac{R_1R_2}{Z_{sc}-R_1-R_3} = \frac{(10E3)^2}{(1E6 - 20E3)} = 102.04 \text{ ohms.} \qquad \text{(Eq. 5.8.1-11)}$$

As can be seen from the example above, no resistance exceeded 10 Kohms but the equivalent 1 Mohms impedance was achieved.

5.8.2 The Problem With Small Capacitors

Stray and parasitic capacitances are two very real problems that exist in every circuit. When a circuit is physically laid out and constructed, relatively small reactances begin to modify the overall circuit performance.

Stay capacitance can be associated with capacitive pick-up between adjacent components or wires. It is primarily a result of the physical layout of module. Usually, stray capacitor can introduce more noise voltage or degrade the stability of a circuit. In a general sense, the impact of stray capacitance is frequency dependent.

Parasitic inductance or capacitance is usually associated with the components used. For small capacities, a parasitic inductance that is associated with the lead length of the capacitors actually translate the capacitor into an inductor at high frequencies beyond the self resonant of the part.

The primary concern for the circuit designer is to be aware of the unforeseen problems associated with the stray and parasitic reactances when designing a circuit. Compensation techniques can in some cases be used to limit their impact.

5.8.3 The Problem With Wide Bandwidth Amplifiers

Many times, the circuit designer thinks in terms of getting the best performance he can from the circuit. This is a very good idea but there are times when less is better. One of those times is when using wide bandwidth amplifiers in audio applications. It is not difficult to understand that if your amplifier needs only to pass audio, then you do not need to pass (amplify) high frequency noise also. Therefore, a simple way to reduce noise in a circuit is to limit the audio amplifier's bandwidth by using a lower bandwidth part.

5.8.4 The Problem With High Gain Stages

High gain amplifier stages have several problems associated with them. First, internal and external noise begins to be a dominant factor. This is why noise filtering should occur prior to high gain stages. Second, many times the designer will not consider amplifier slew rate. Remember that slew rate is a measured in Volts/usec and is limited by the bandwidth of the amplifier. Third, the higher the gain bandwidth product, the more likely you will design and build an unstable stage. As the gain of an amplifier stage increases, more phase/frequency compensation is needed to ensure that the stage is stable.

5.9 DOCUMENTATION AND REVIEWS

There is a preferred avenue for retaining design notes, test results, etc., relative to your work. An Engineering Notebook can provide a consolidated record for future reference. It is important for you to retain records on the things you have worked on. Telephone conversations with outside vendors or agencies can be recorded on Form FW ITT g-15. Regardless of how you keep your notes, you should be able to produce reasonable documentation on the projects you have worked on. Reasonable documentation should include design equations, assumptions, test results and plans, memos or reports you have written, schematics, and all notes which are original to you or have been given to you as originals. At present, the analog circuit designer in the Analog Design Section is required to submit a bi-weekly highlight to the project engineer(s) and section head.

Circuit design does not preclude circuit analysis. Each circuit that you include in a design should include a circuit origin. If a circuit is "cut and pasted" from an existing system, there should be more than an educated guess as to how it works. If the circuit is from an application note or text book, that does not mean that all possible implementations of the circuit have been considered. The type and amount of circuit analysis should also be based on meeting the desired performance requirements. Notes relative to the circuit analysis should be maintained and well documented.

During the course of the design, there will be numerous formal and informal design reviews in which the circuit designer will participate. Design reviews should include adequate technical detail so that the majority of technical issues can be answered at the review. Transfer functions, Bode plots, worst case analysis, etc., should be presented if the electrical engineer is proving that the circuit works on paper, is looking for technical direction, or wants to relax or change the performance requirements. Design review notes should be available and distributed before the design review.

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