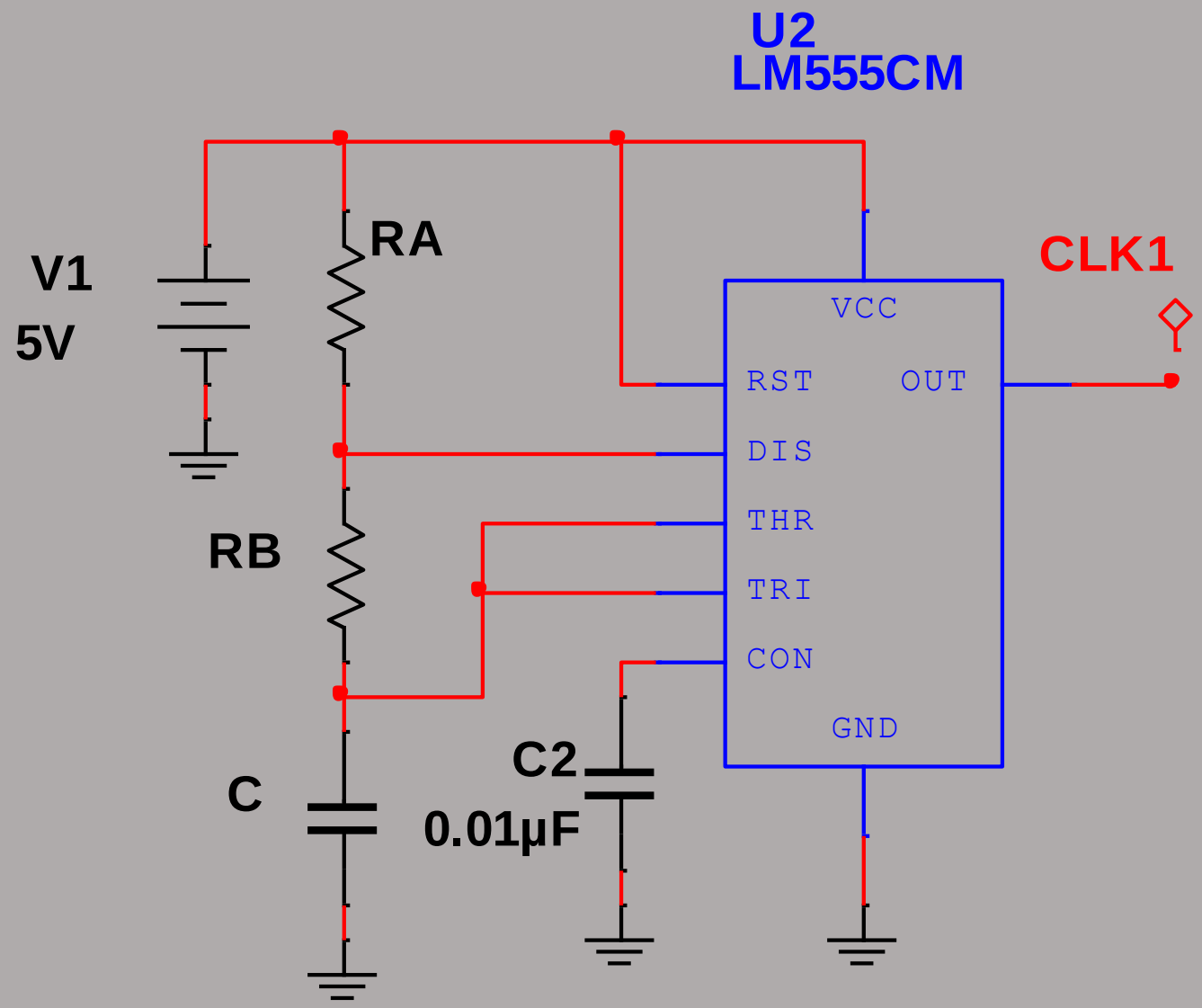
EECT 122 spring 2020

Brian Yang, Morgan Wilcox, and also with
Miles Sierk During distance learning

Professor: Mr. Bell

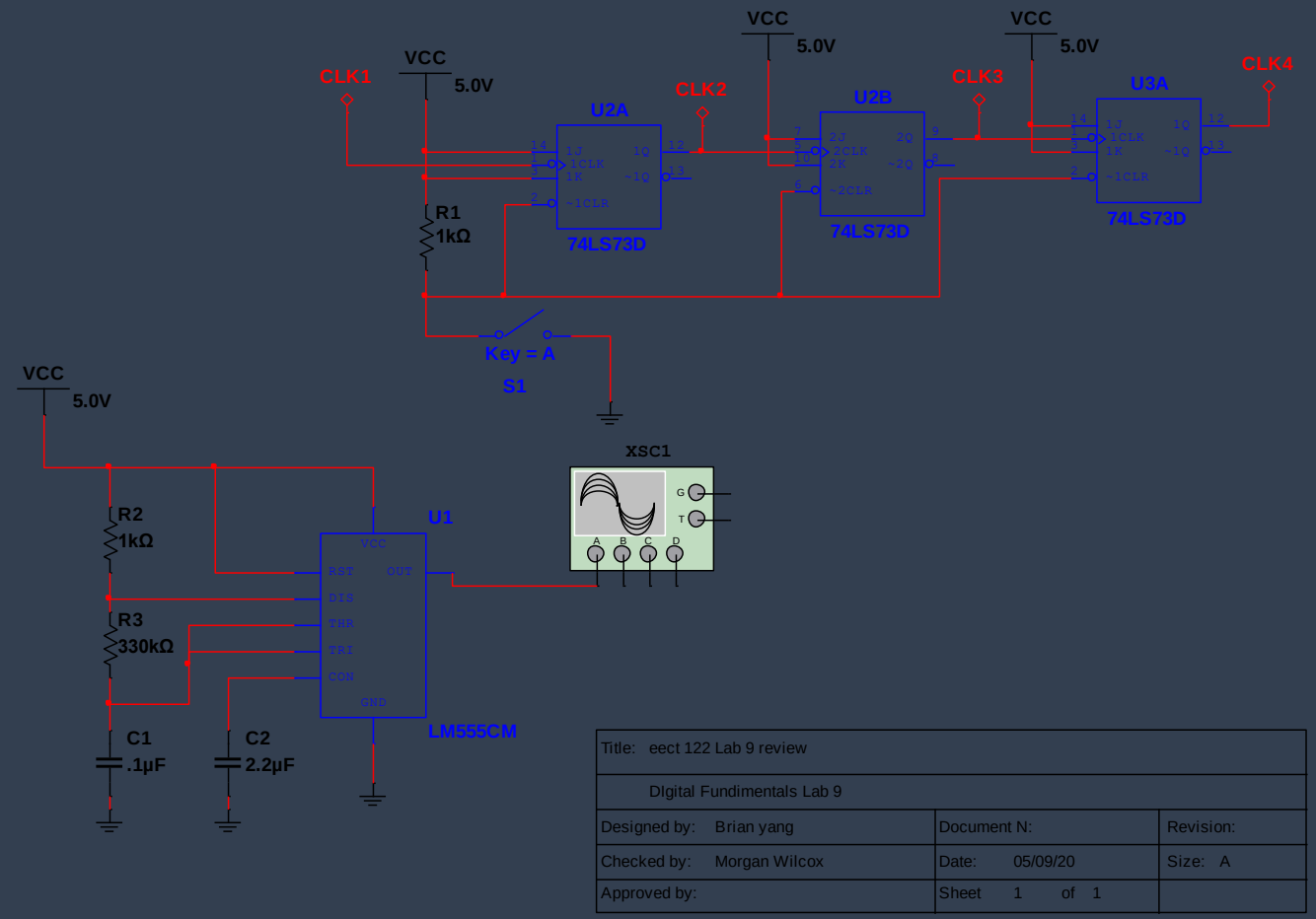
EECT 122 table of content

Lab 9 redo


U2
LM555CM
V1
5V
RA
RB
C
C2
0.01µF
CLK1
VCC
RST
OUT
DIS
THR
TRI
CON
GND

Objective

- The purpose of this lab is to:
- Many times you can use multiple harmonically related clocks to test a combinational circuits. The Purpose of this lab is to show students how to create a small multiple clock counter circuit that uses JK Flip Flops and a 555 Timer



Title: eect 122 Lab 9 review		
DIgital Fundimentals Lab 9		
Designed by: Brian yang	Document N:	Revision:
Checked by: Morgan Wilcox	Date: 05/09/20	Size: A
Approved by:	Sheet 1 of 1	

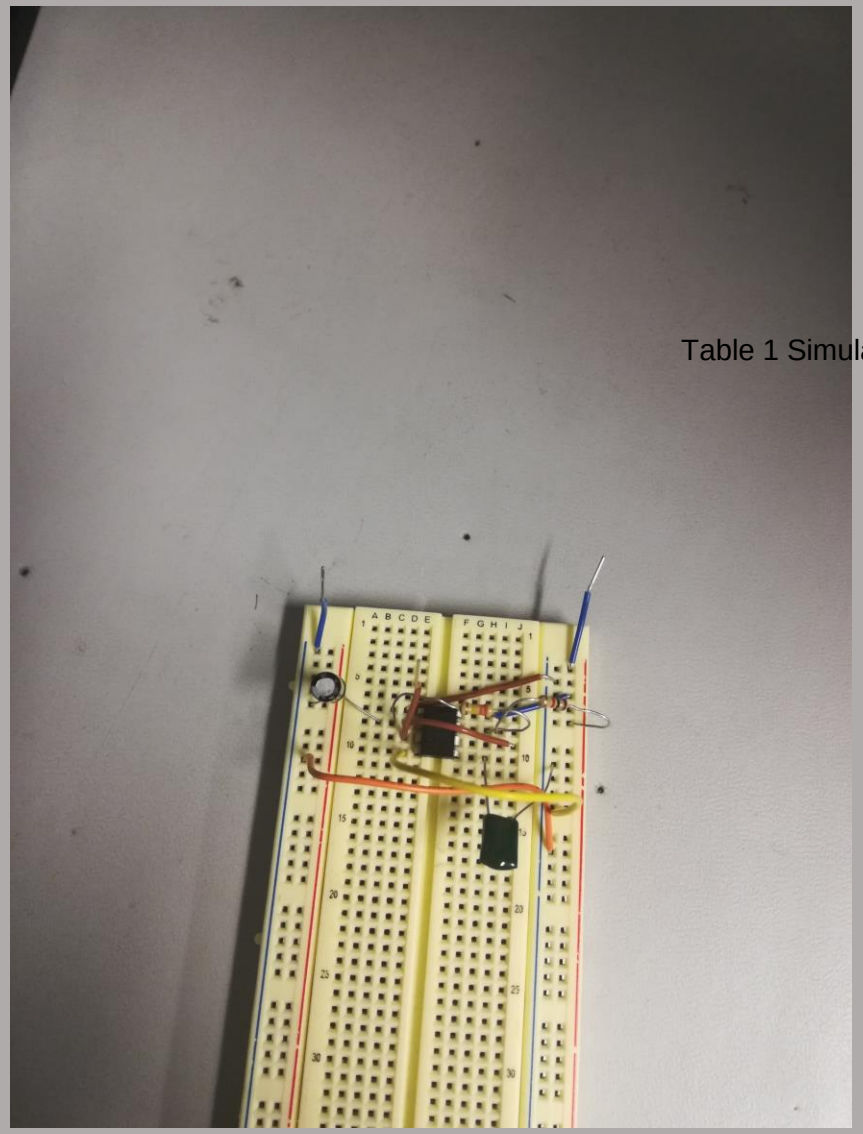
Equipment needed

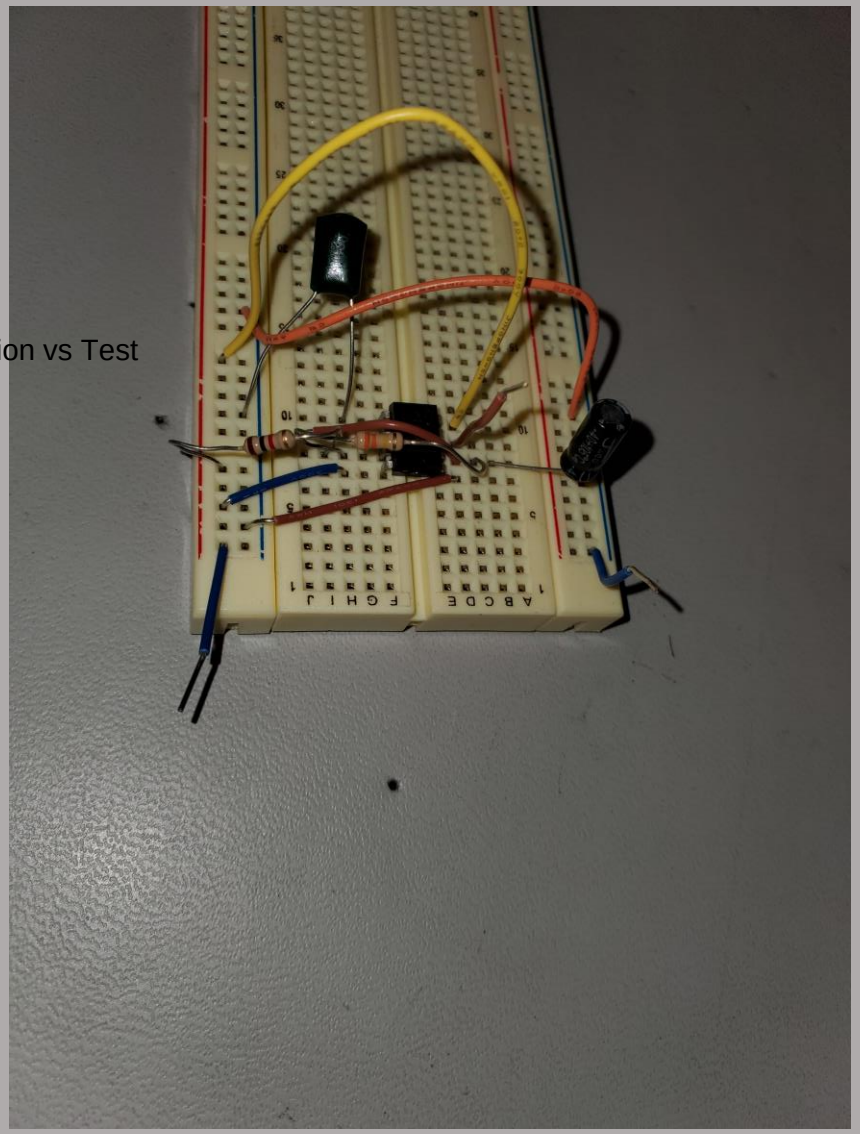
- 1 – 555 Timer
- 1 – 1Kohm
- 1 – 4 position dip switch
- 2 – 74LS73 Dual JK flip flop
- 2 – Resistors (To Be Designed)
- 2 – Capacitors (To Be Designed)

Lab 9 redo

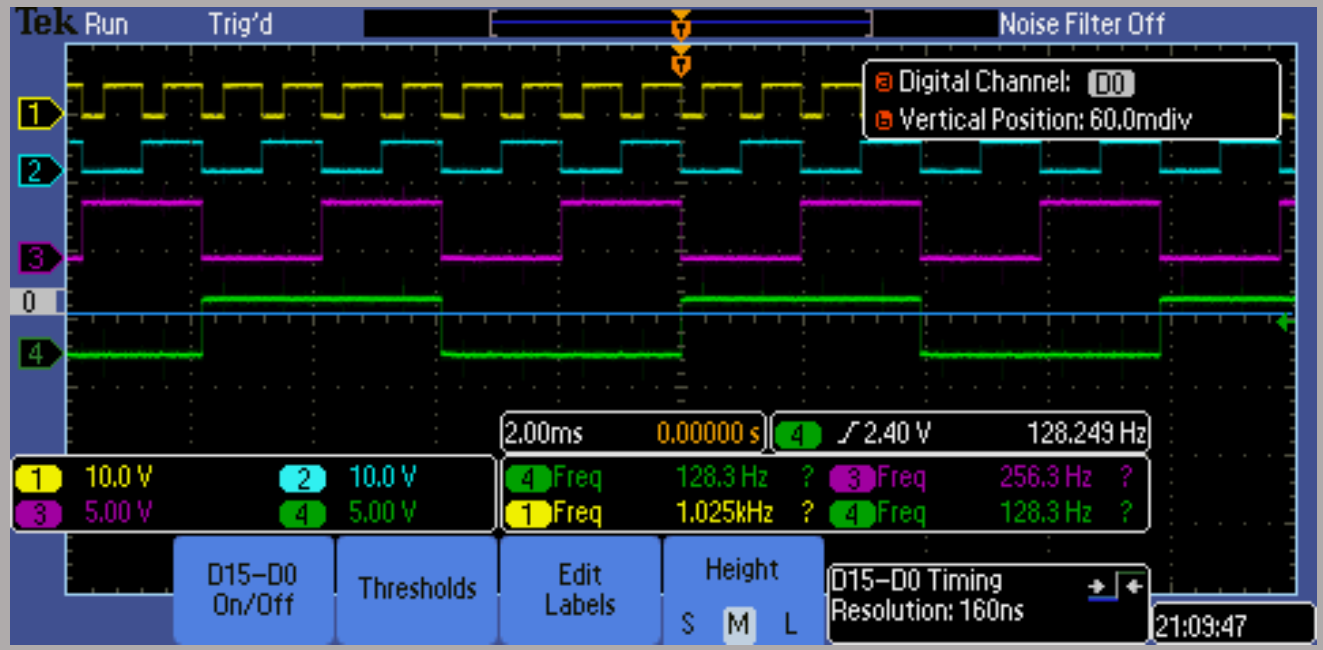
	Designed	Measured
R_A =	1kΩ	1.003kΩ
R_B =	330kΩ	332.4kΩ
C =	2.2uF	2.352uF
t_1 =	128.095ms	
t_2 =	1.139s	
T =	1.011s	1.120s
f =	0.9923Hz	
D =	49.9%	

Table 1 Simulation vs Test





Ra	1000
Rb	330,000
C	2.2uf
t1	1.594
t2	2.643
t	1.048
f	500mv
D	0.49924



observations

- Initially we thought we had a bad breadboard but we just didn't wire the 74ls73 up properly. Our reading were within acceptable range of the calculations and multi sim. Overall it was much more simple the second time doing it.

Alt Gates

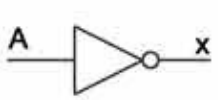
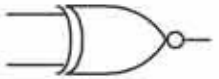

AND
A
B
A · B
A
B
$\overline{\bar{A} + \bar{B}} = AB$


OR
A
B
A + B
A
B
$\overline{\bar{A} \cdot \bar{B}} = A + B$


NAND
A
B
$\overline{AB}$
A
B
$\bar{A} + \bar{B} = \overline{AB}$


NOR
A
B
$\overline{A + B}$
A
B
$\bar{A} \cdot \bar{B} = \overline{A + B}$

Logic Gates

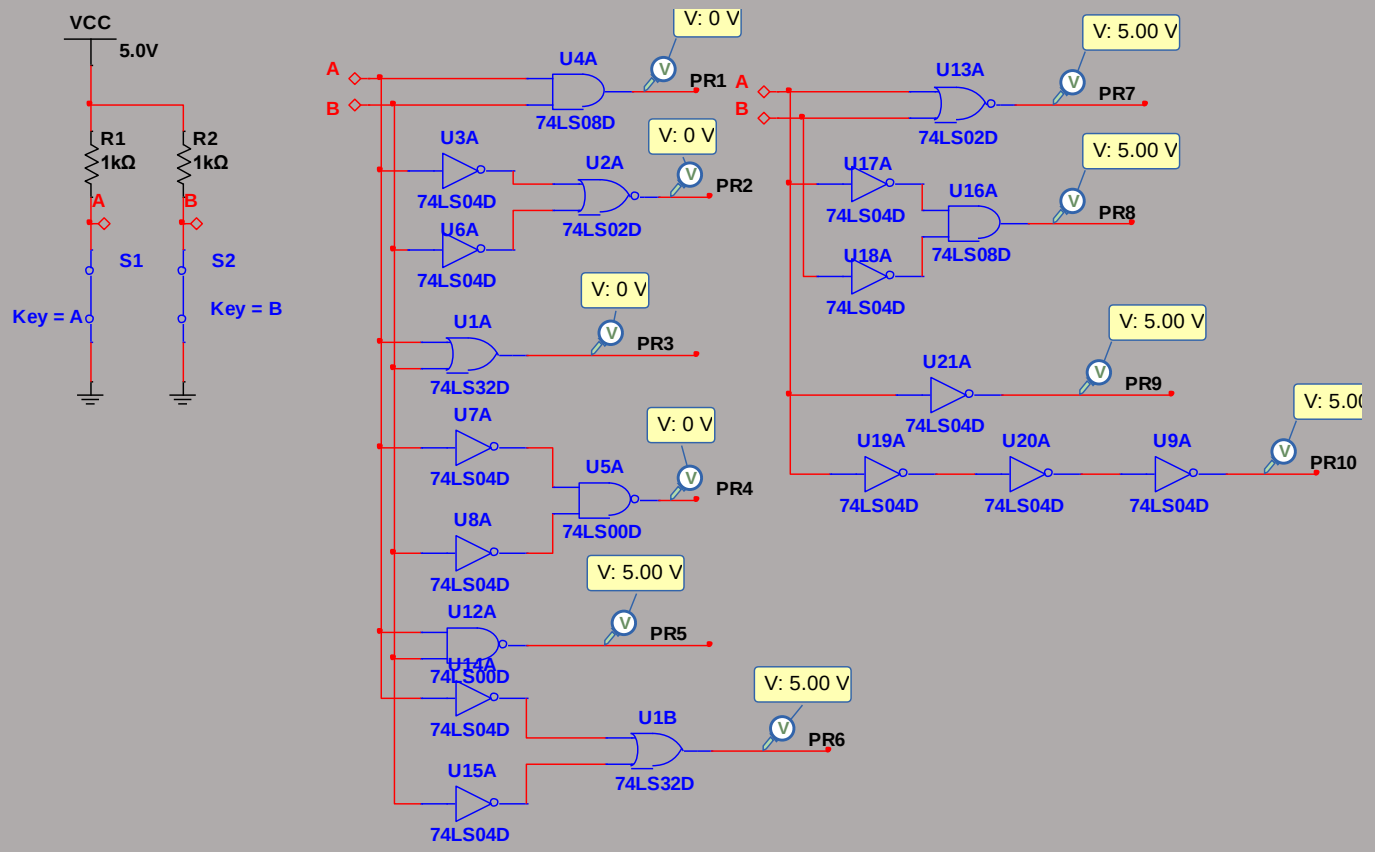
Name	NOT	AND	NAND	OR	NOR	XOR	XNOR
Alg. Expr.	$\overline{A}$	AB	$\overline{AB}$	$A+B$	$\overline{A+B}$	$A \oplus B$	$\overline{A \oplus B}$
Symbol							
Truth Table	A | X 0 | 1 1 | 0	B A | X 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1	B A | X 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0	B A | X 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1	B A | X 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0	B A | X 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 0	B A | X 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 1

Alt Gate

Objective

- Build and test the alt gates with standard and alternative structure
- Invert each input and output in standard symbols

Alt gates


VCC
5.0V
R1
1kΩ
R2
1kΩ
A
B
S1
S2
Key = A
Key = B
A
B
U4A
74LS08D
V: 0 V
PR1
U3A
74LS04D
U2A
74LS02D
V: 0 V
PR2
U6A
74LS04D
V: 0 V
U1A
74LS32D
PR3
U7A
74LS04D
U5A
74LS00D
V: 0 V
PR4
U8A
74LS04D
V: 5.00 V
U12A
PR5
U14A
74LS00D
74LS04D
U1B
74LS32D
V: 5.00 V
PR6
U15A
74LS04D
A
B
U13A
74LS02D
V: 5.00 V
PR7
U17A
74LS04D
U16A
74LS08D
V: 5.00 V
PR8
U18A
74LS04D
V: 5.00 V
U21A
74LS04D
PR9
U19A
74LS04D
U20A
74LS04D
U9A
74LS04D
V: 5.0
PR10

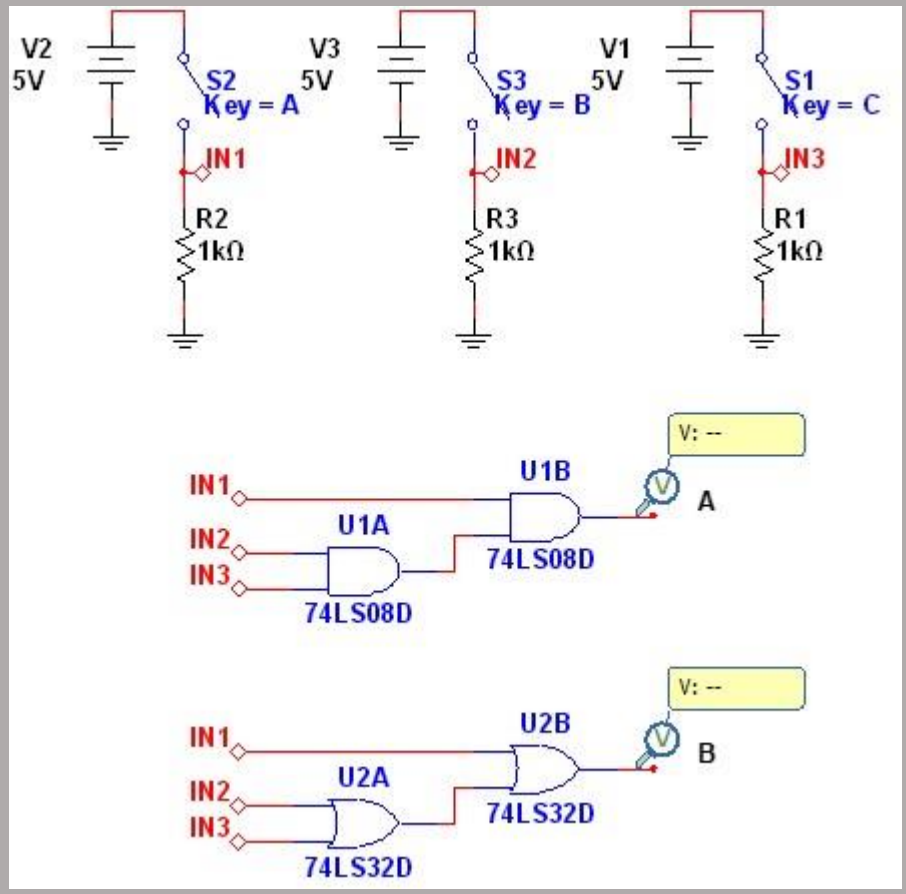
Alt gate

Observations

We initially tested it but didn’t get any readings when we flipped a switch so I checked the dipswitch and we had grabbed one that didn’t stay in our board very well (has little notches on underside). We switched it out for one that didn’t and it functioned afterward

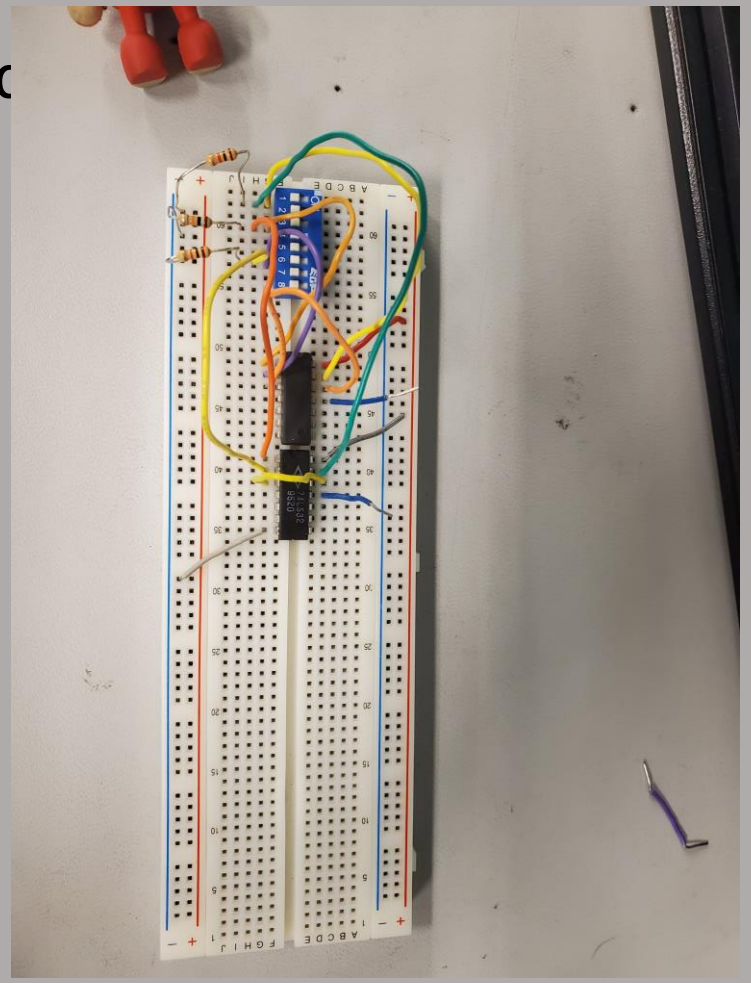
Build you own lab

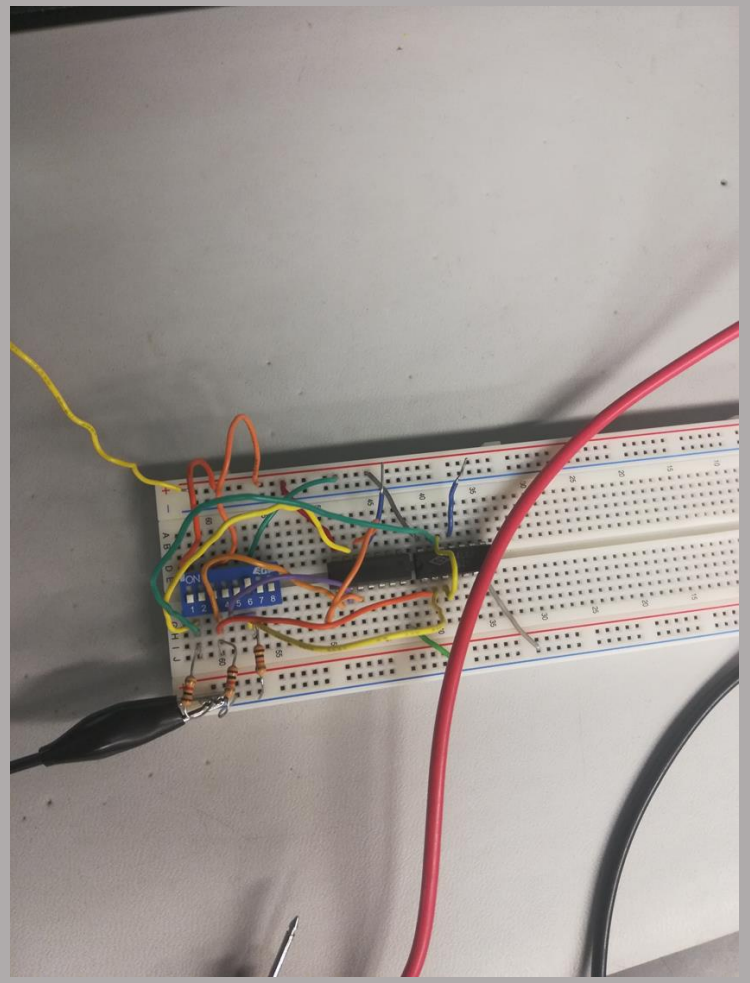
- The purpose of this lab is to:
- Check the AND / OR outputs with DMM



Equipment needed

- Equipment & parts needed
- BREADBOARD
- 3, 1K OHM RESISTOR
- 1, 74LS08D
- 1, 74LS32D
- DIP SWITCH
- DC POWER SUPPLY
- DMM
- WIRES
- DATA SHEETS





Build your own lab

DESIGN	SIMULATED	TEST
1K RESISTOR	1KOHM	0.9838 KOHM
1K RESISTOR	1KOHM	0.9854 KOHM
1K RESISTOR	1KOHM	0.9895 KOHM

DESIGNED TRUTH TABLE

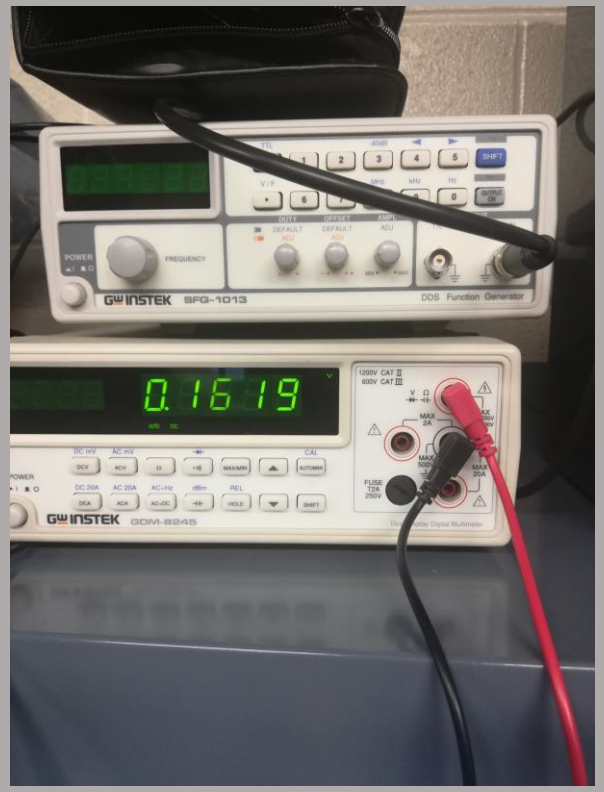
A	B	C	And Outputs	Or Outputs
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

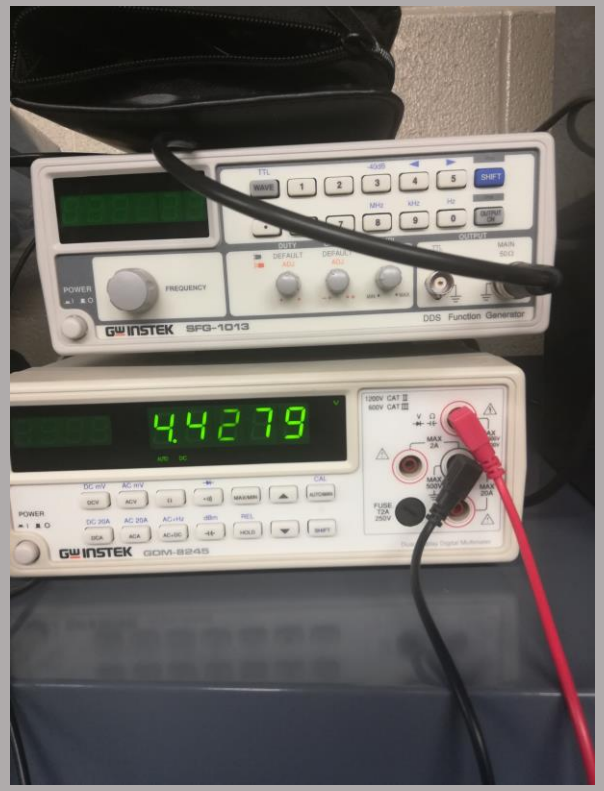
TESTED TRUTH TABLE

A	B	C	And Outputs	Or Outputs
0V	0V	0V	0.1619V	0.1508V
0V	0V	5V	0.1619V	4.4622V
0V	5V	0V	0.1619V	4.4622V
0V	5V	5V	0.1619V	4.4622V
5V	0V	0V	0.1619V	4.4622V
5V	0V	5V	0.1619V	4.4622V
5V	5V	0V	0.1619V	4.4622V
5V	5V	5V	4.4279V	4.4622V

Build your own lab

AND





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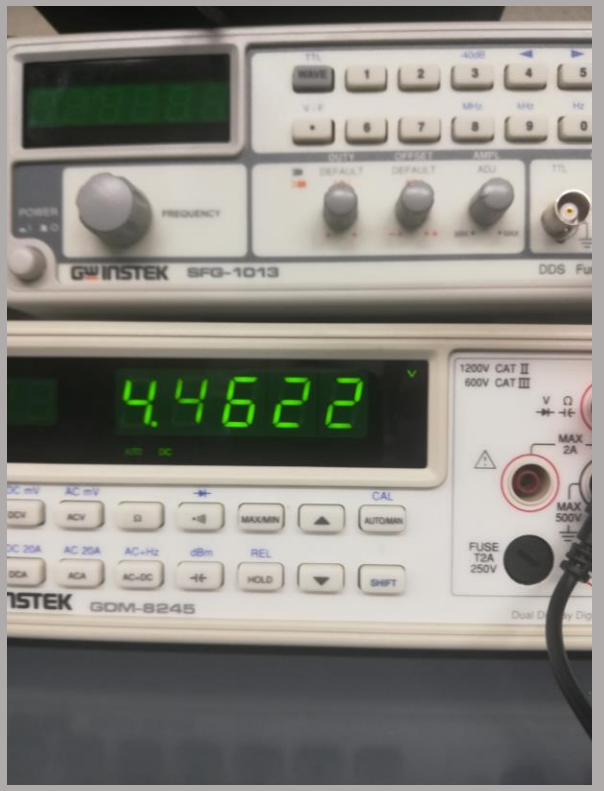


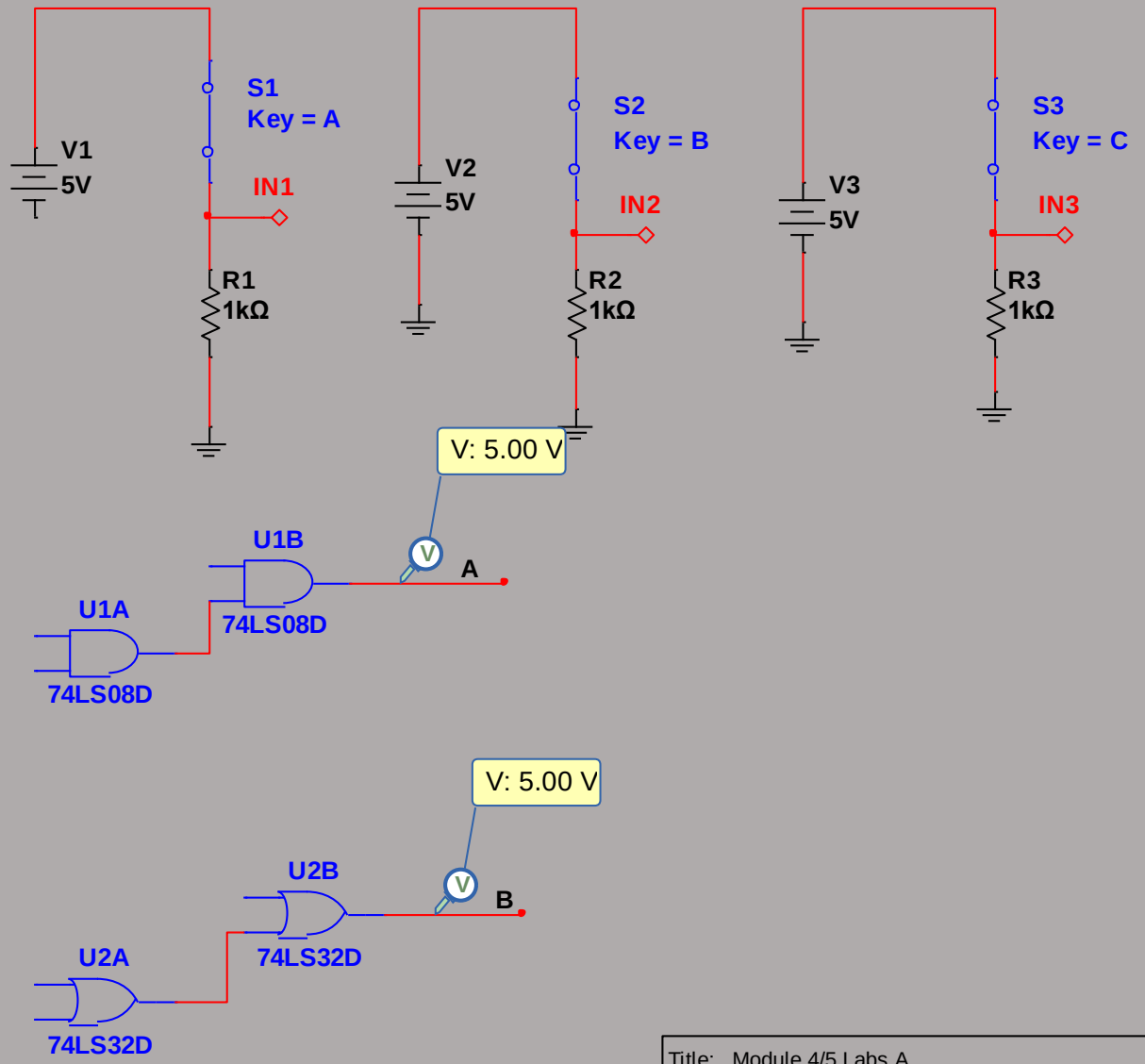
Observations

- We had to double check data sheets to make sure layout was correct, we also accidently had a 10k ohm resistor thinking it was a 1k (red vs orange) in our build we caught it before we ran power to it. All reading were what we expected and within acceptable figures. And comparable to the multi sim readings.

Mod 5 Labs 1-10

- Lab 1
- Lab 2 NAND Latch
- Lab 3 SR Flip Flop
- Lab 4 D Flip Flop
- Lab 5 JK Flip Flop
- Lab 6 2’s Compliment
- Lab 7 4 Bit Adder
- Lab 8 Asynchronous Counter
- Lab 9 Synchronous Counter
- Lab 10 Mod 12 Synchronous Counter

Lab 1



Title: Module 4/5 Labs A		
LAB 1		
Designed by: brian yang	Document N:	Revision:
Checked by:	Date: 2/6/2020	Size: A
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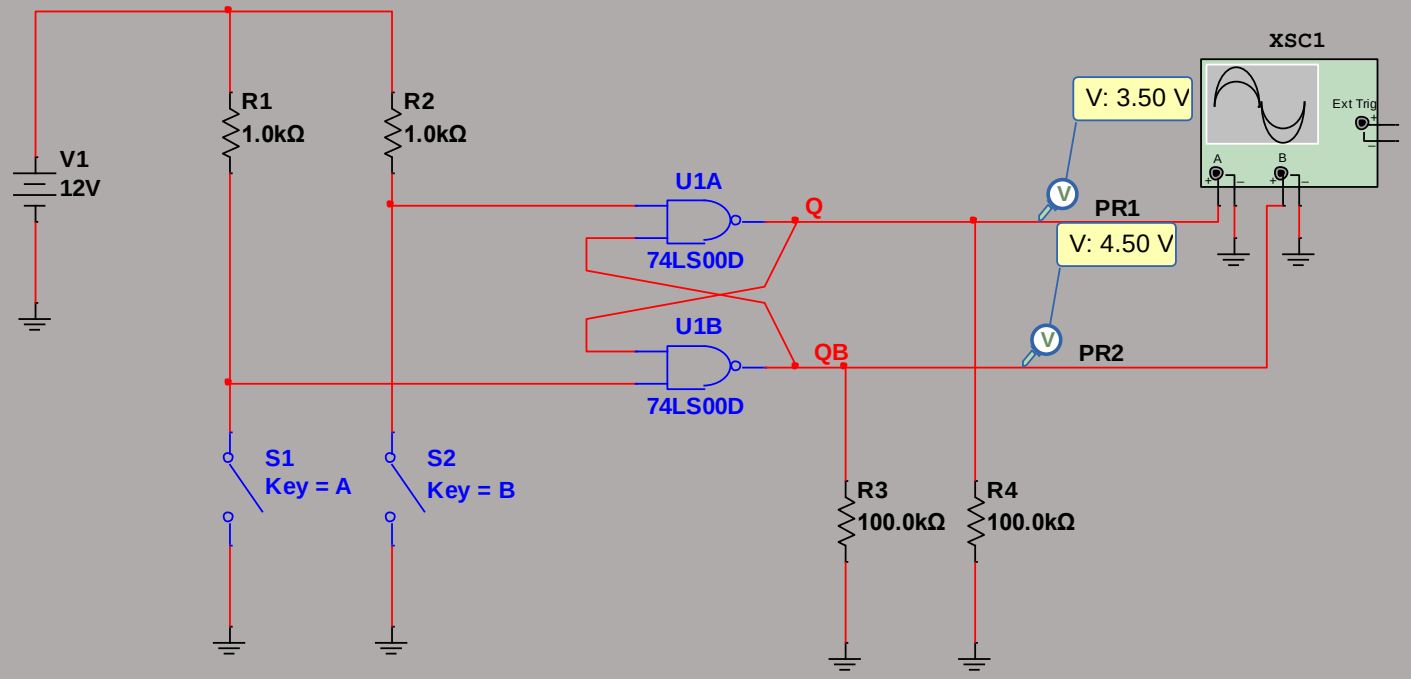
Lab 2 NAND Latch



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Lab 2		
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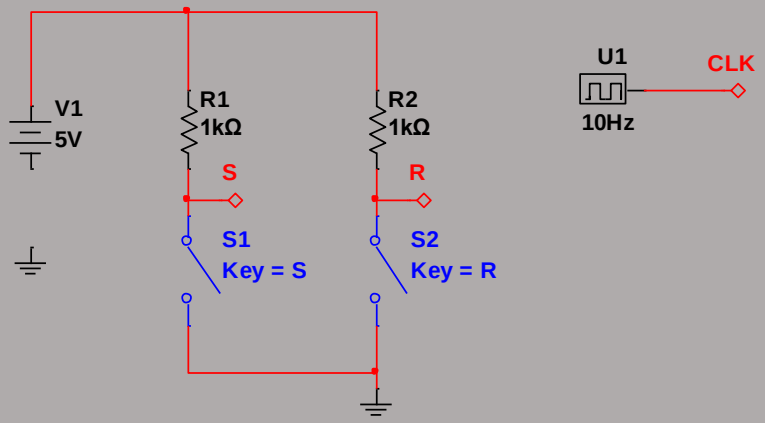
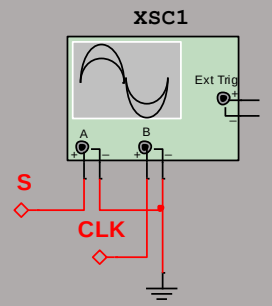
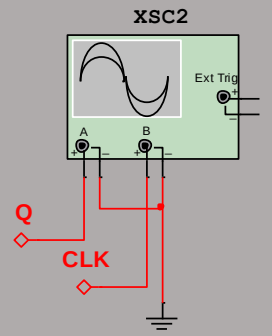
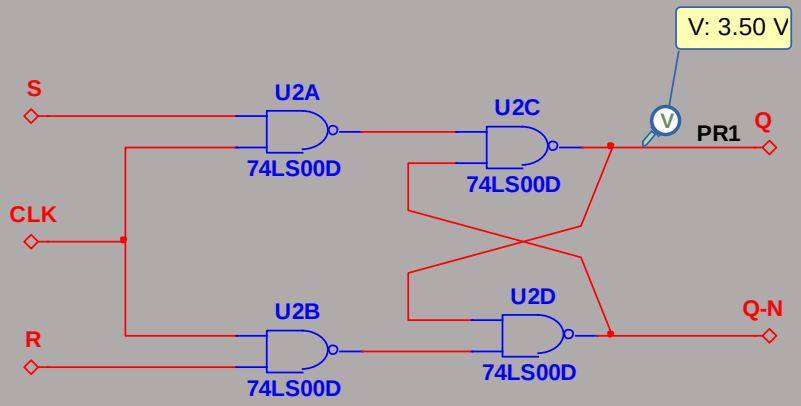
Lab 3 SR Flip Flop









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Lab 3 - SR Flip Flop		
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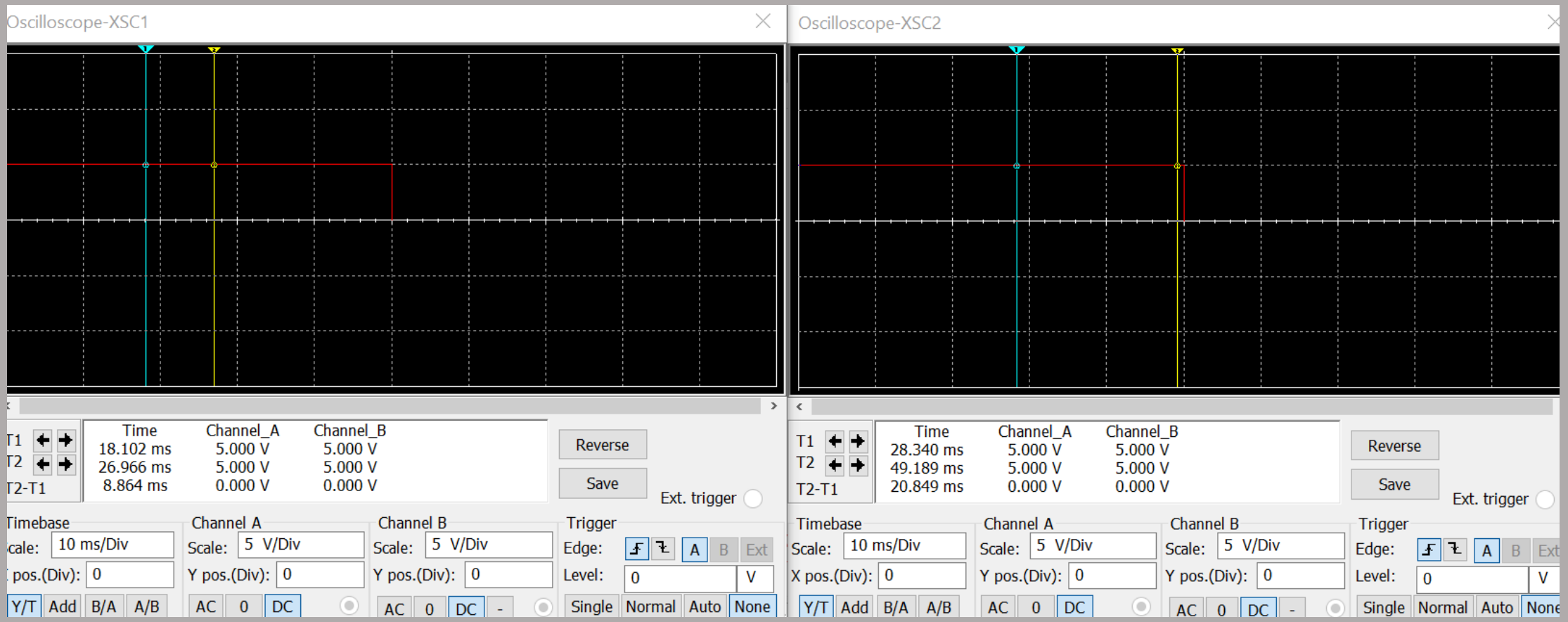
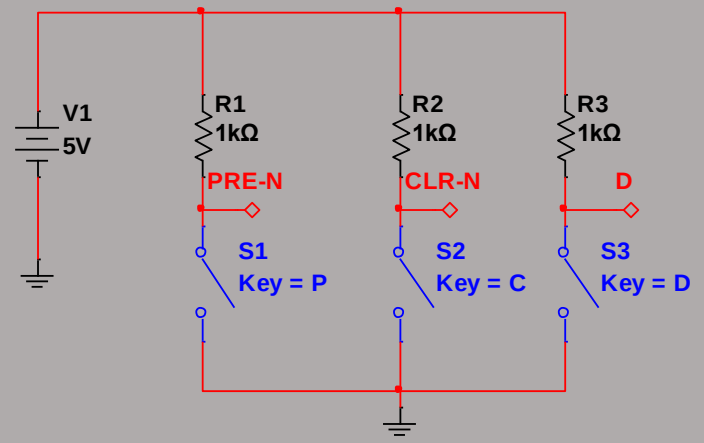
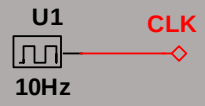
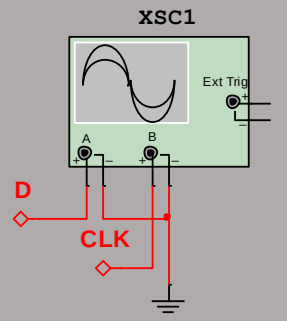
Lab 3 SR Flip Flop

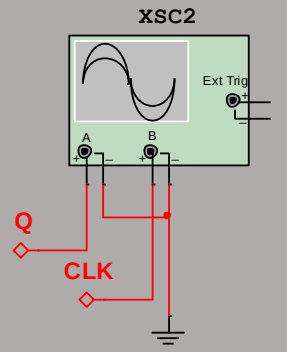


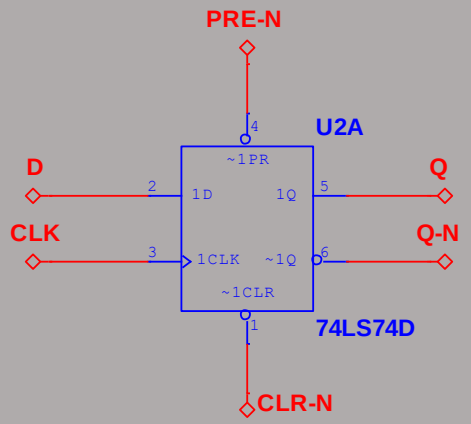
Lab 4 D Flip Flop











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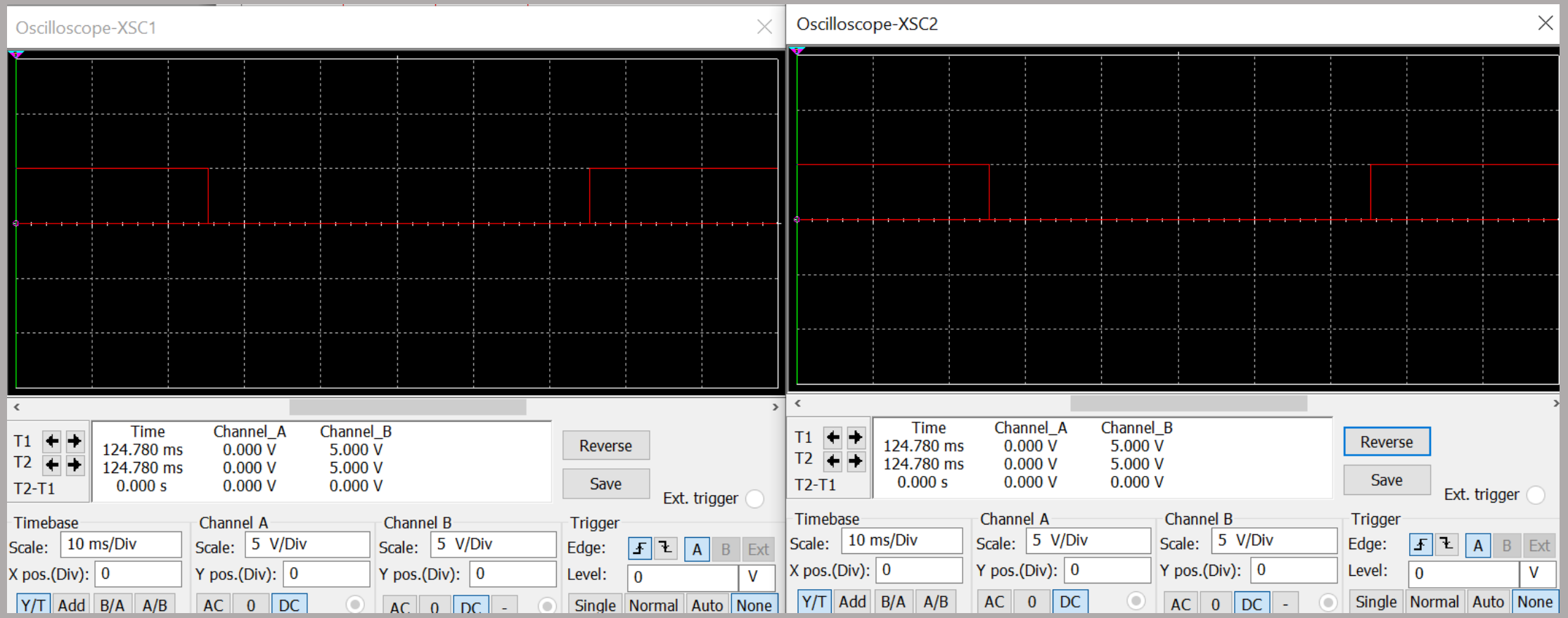
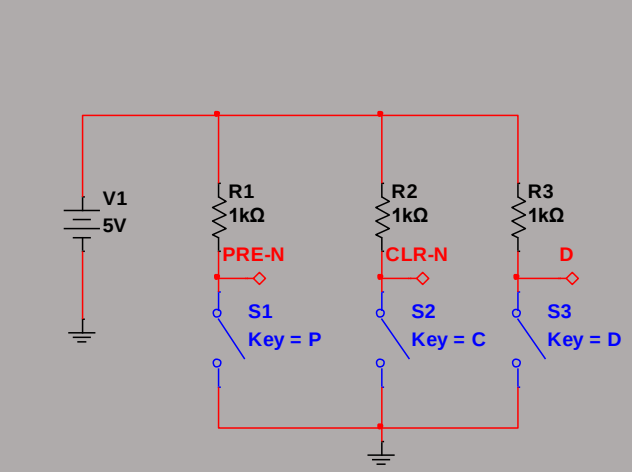
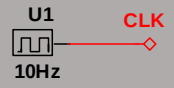
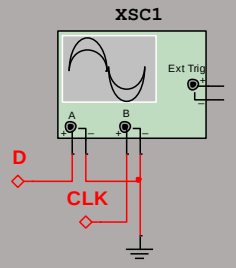
Lab 4 D Flip Flop

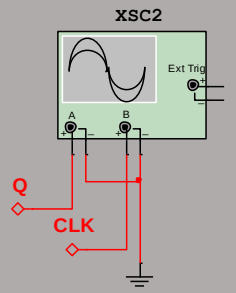


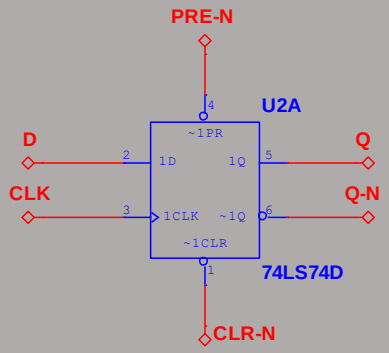
Lab 5 JK Flip Flop











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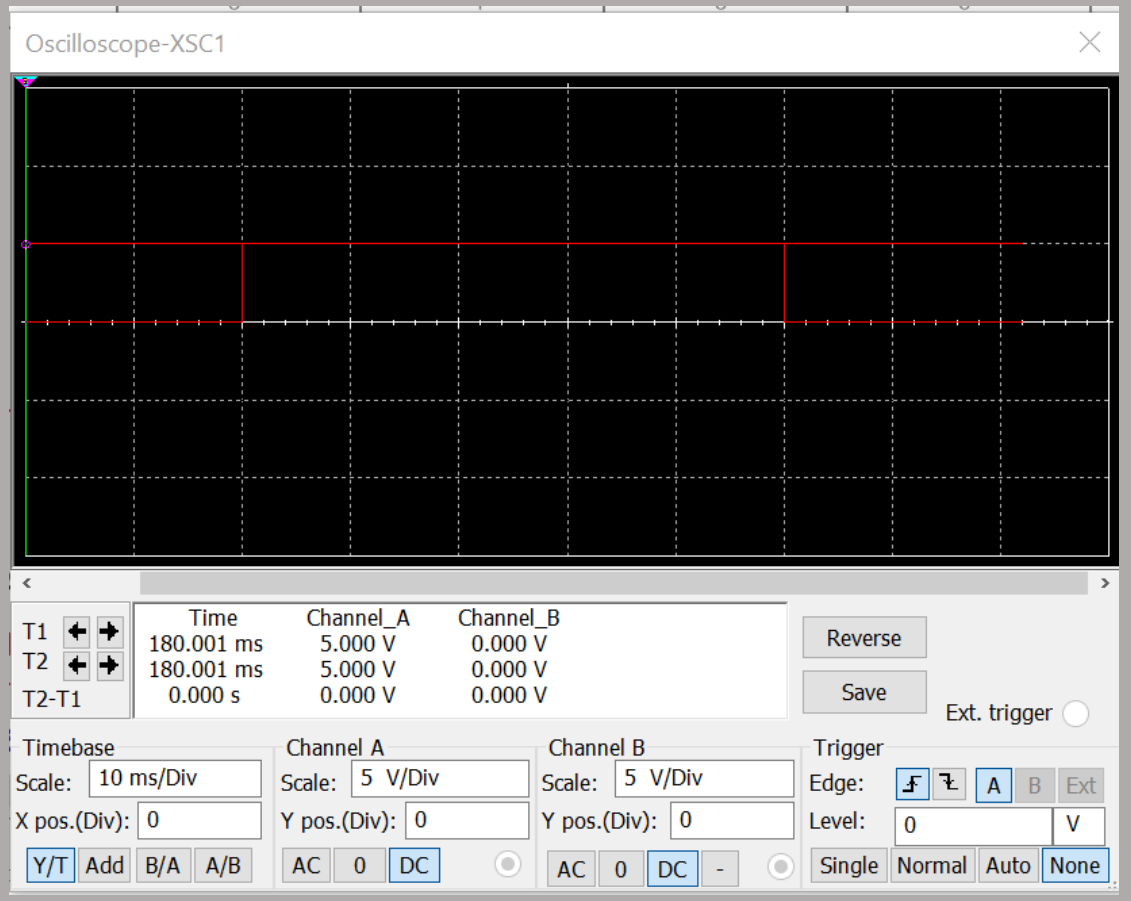
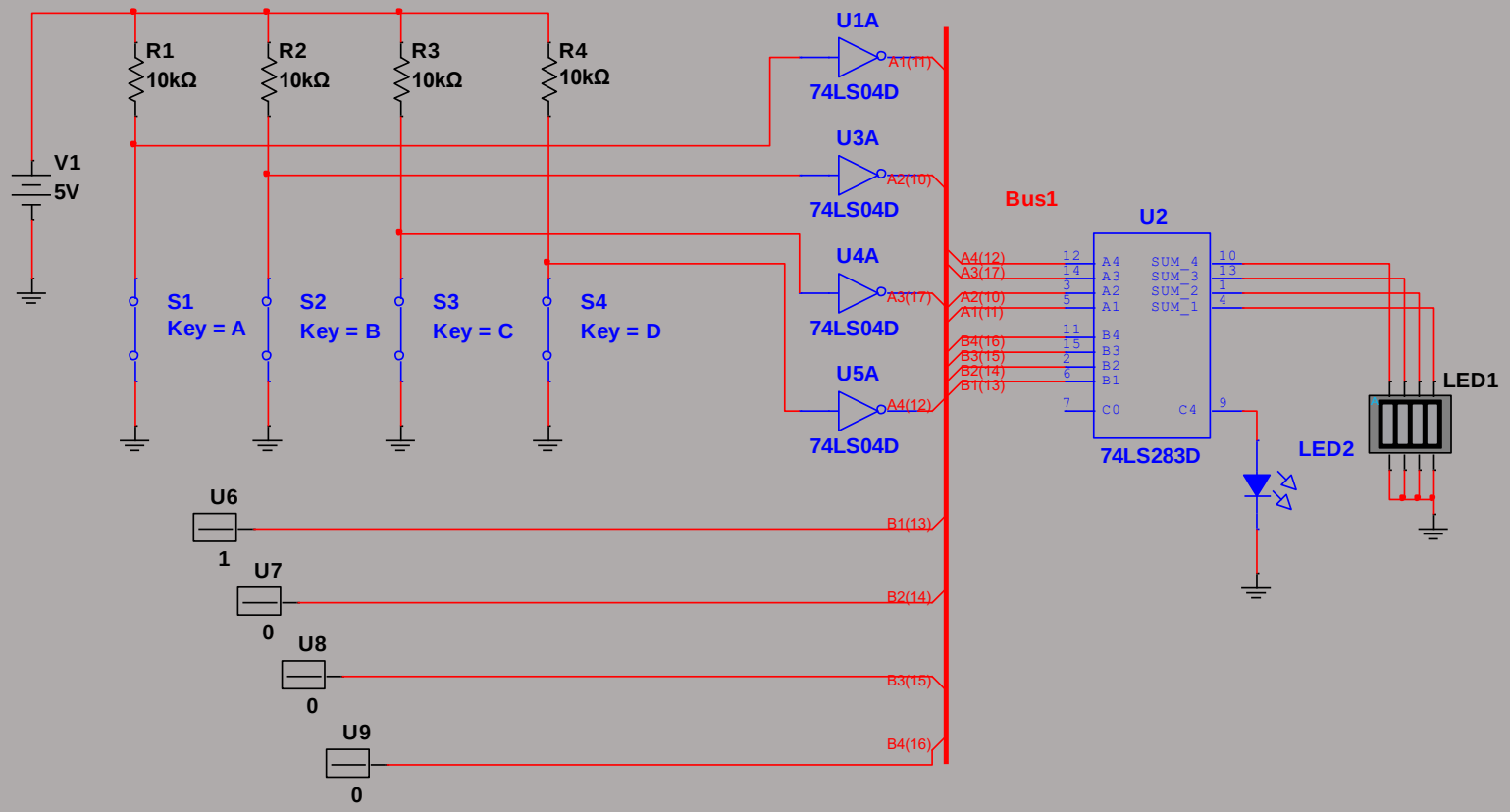


Lab 6 2's Compliment



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Lab 5 - 2's Complement		
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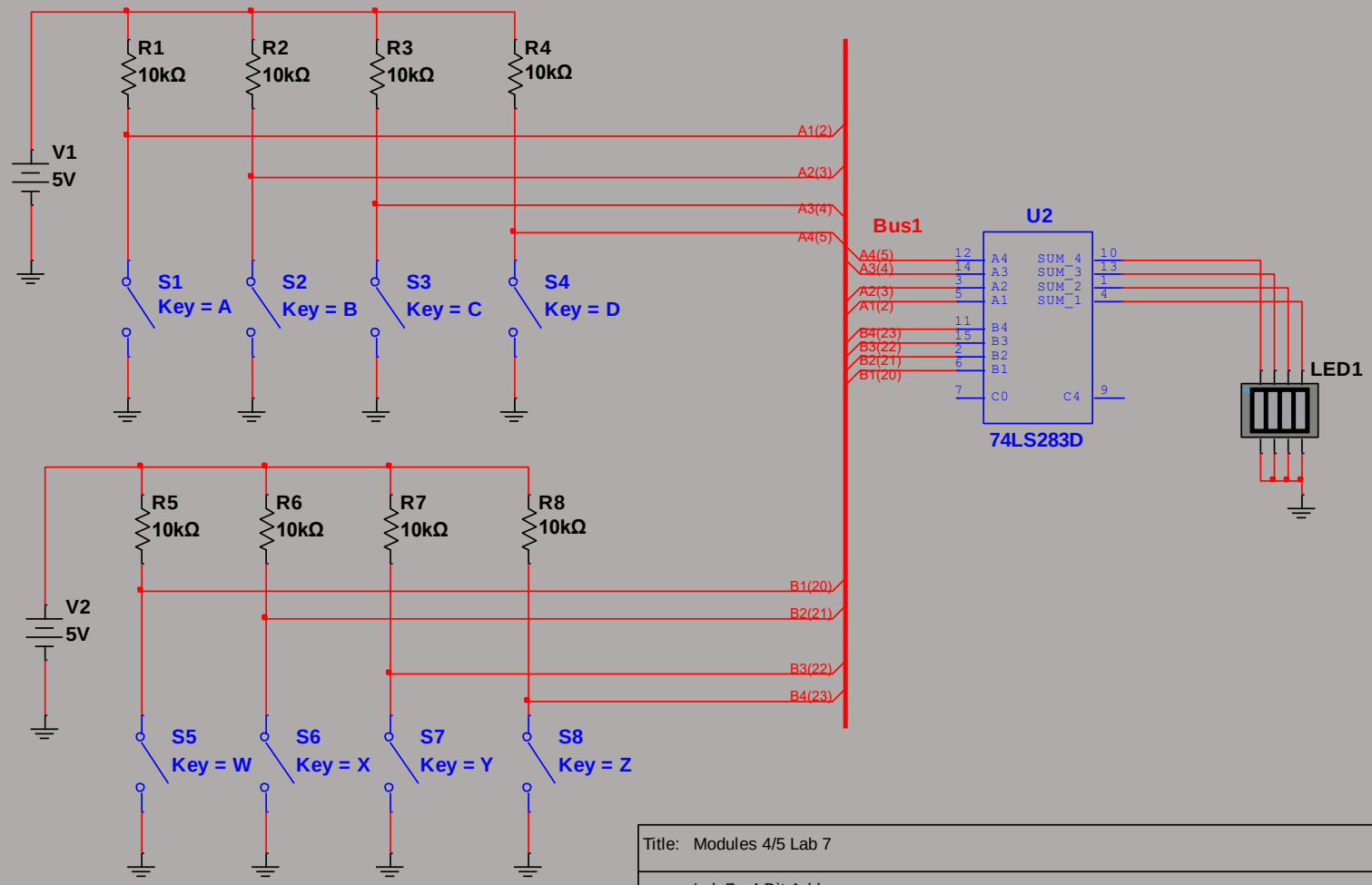
Lab 7 4 bit Adder



Title: Modules 4/5 Lab 7		
Lab 7 - 4 Bit Adder		
Designed by: brian yang	Document N:	Revision:
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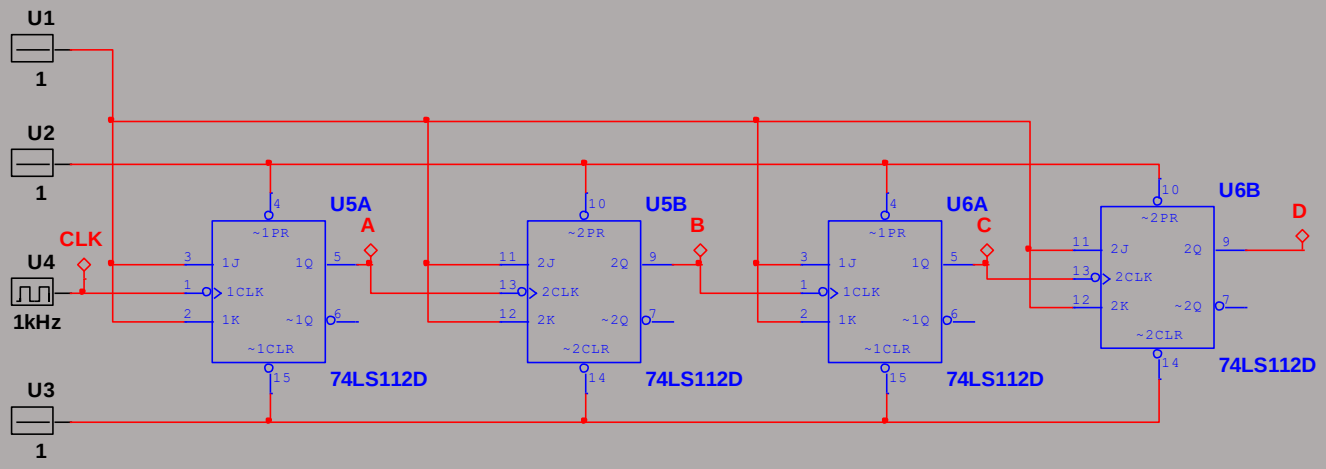
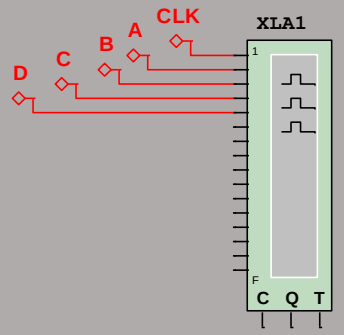
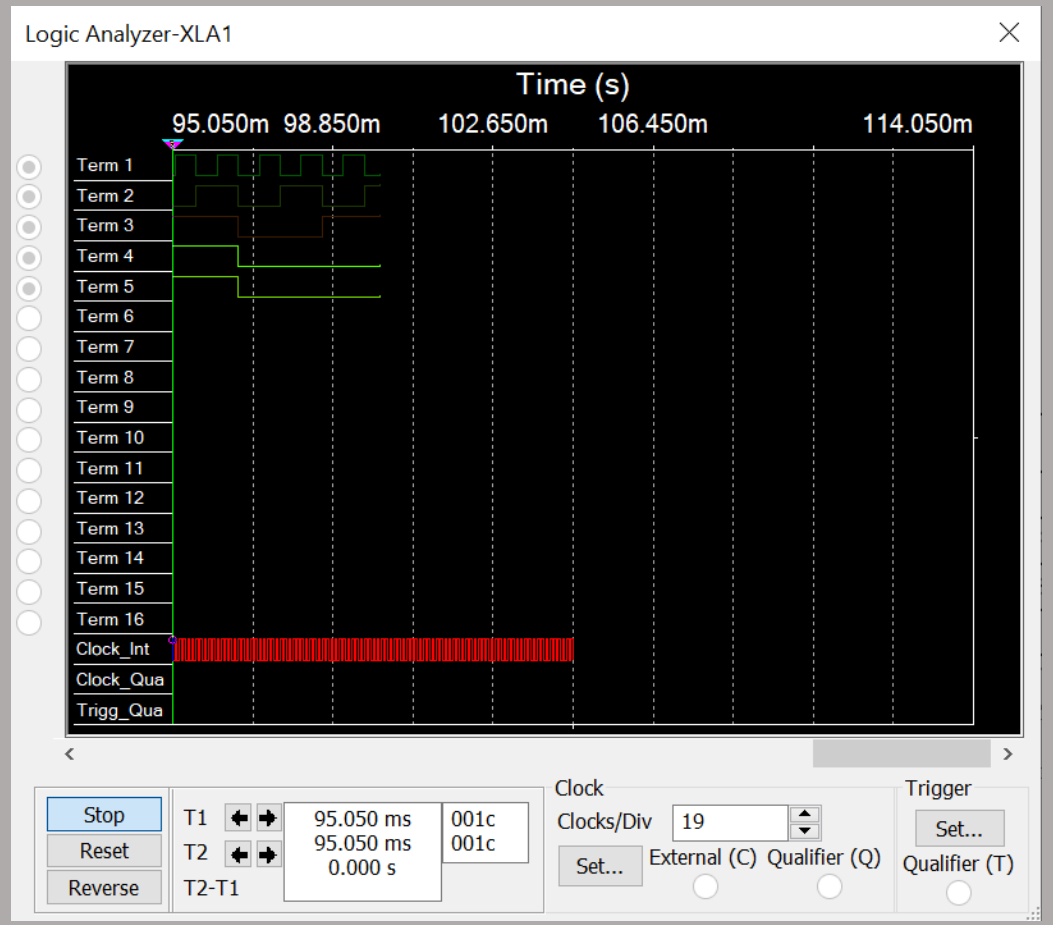
Lab 8 Asynchronous Counter







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Lab 8 - Asynchronous Counter		
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Checked by:	Date: 2/7/2020	Size: A
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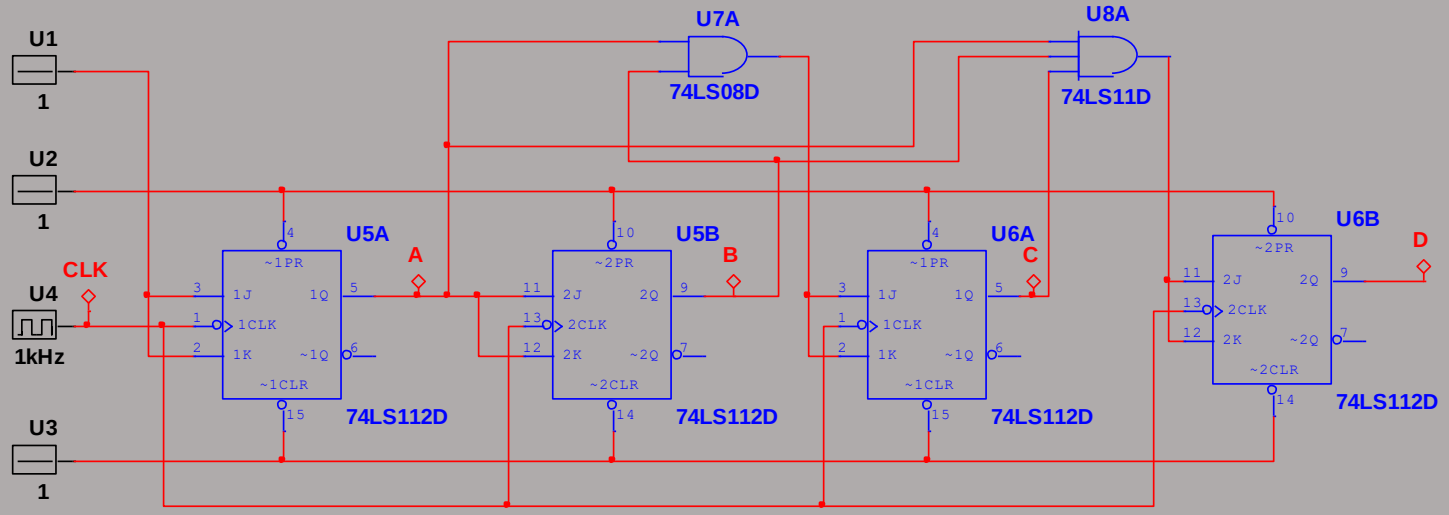
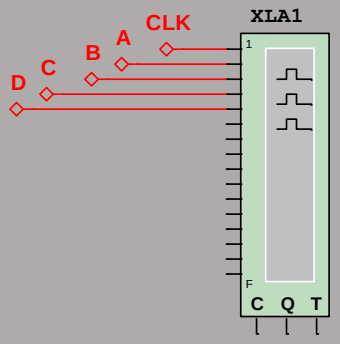
Lab 9 Synchronous Counter





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Lab 9 - Synchronous Counter		
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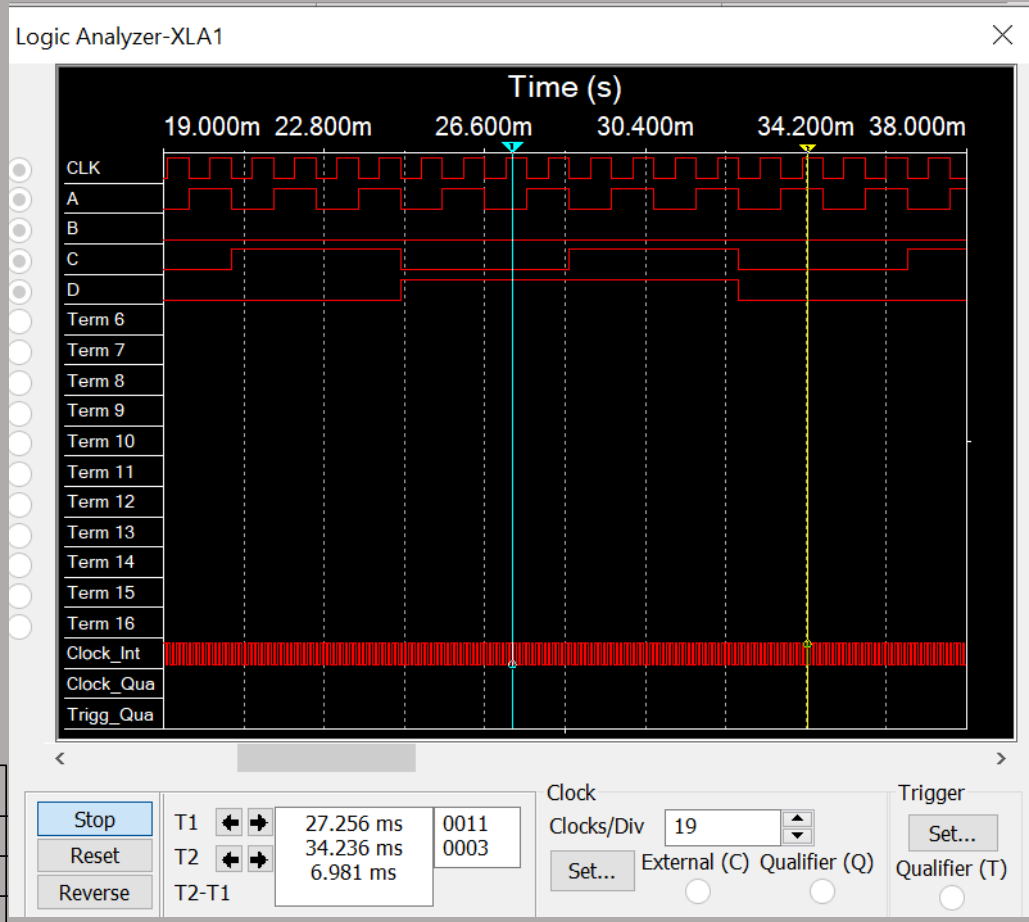
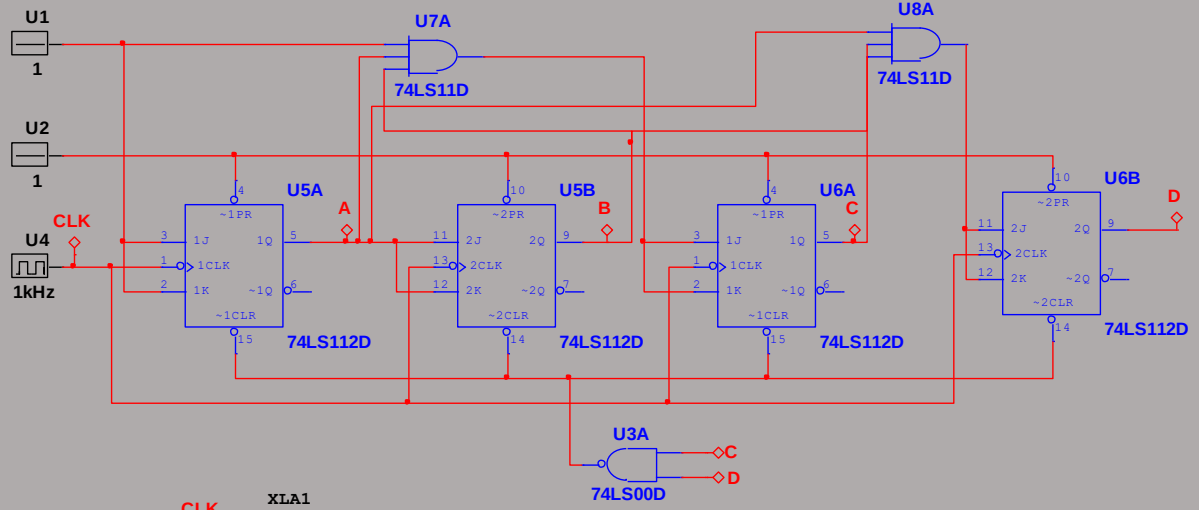
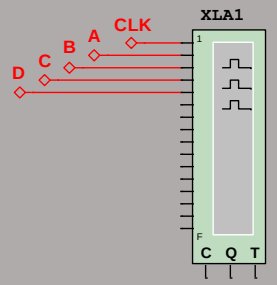
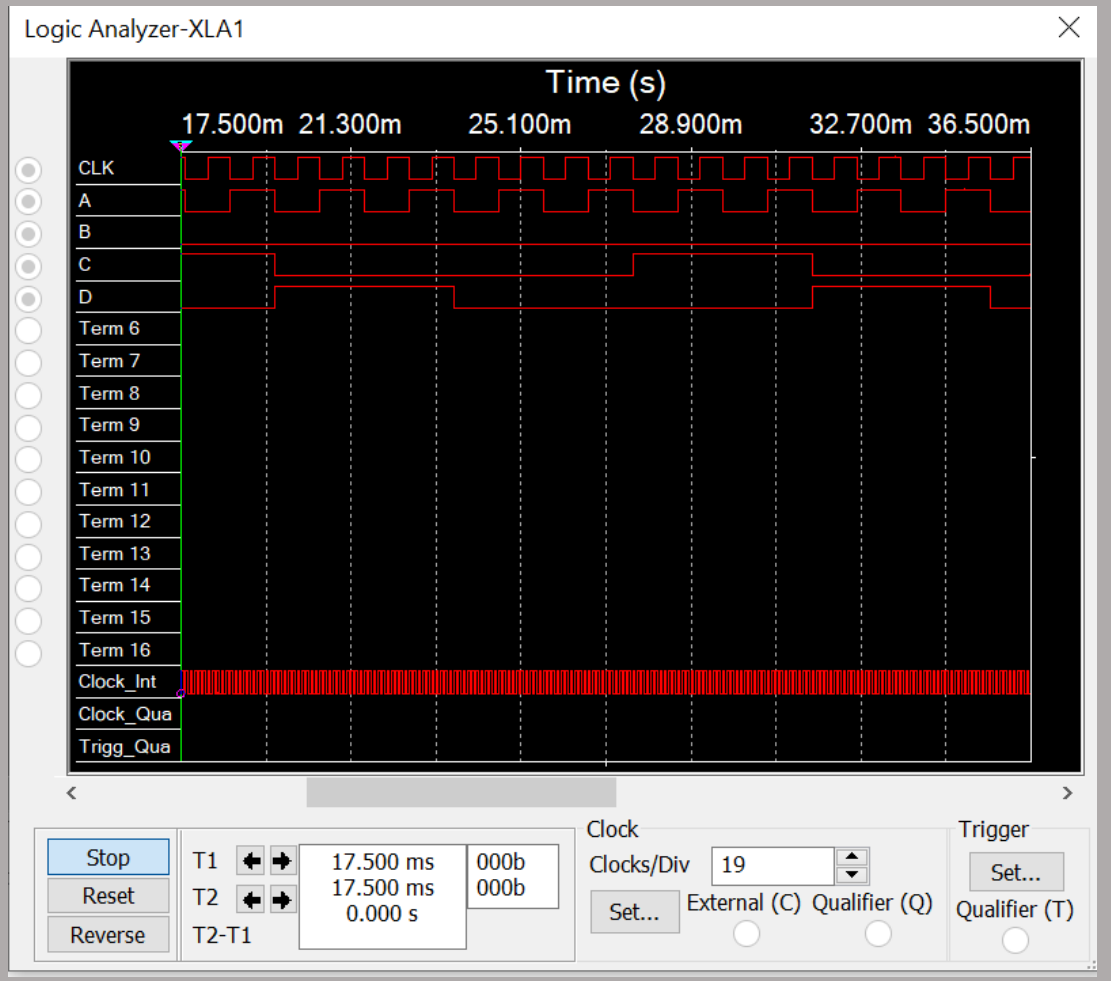


Lab 10 Mod 12 Synchronous Counter





Title: Module 4/5 Lab 10		
Lab 10 - mod 12 Synchronous Counter		
Designed by: brian yang	Document N:	Revision:
Checked by:	Date: 2/7/2020	Size: A
Approved by:	Sheet 1 of 1	



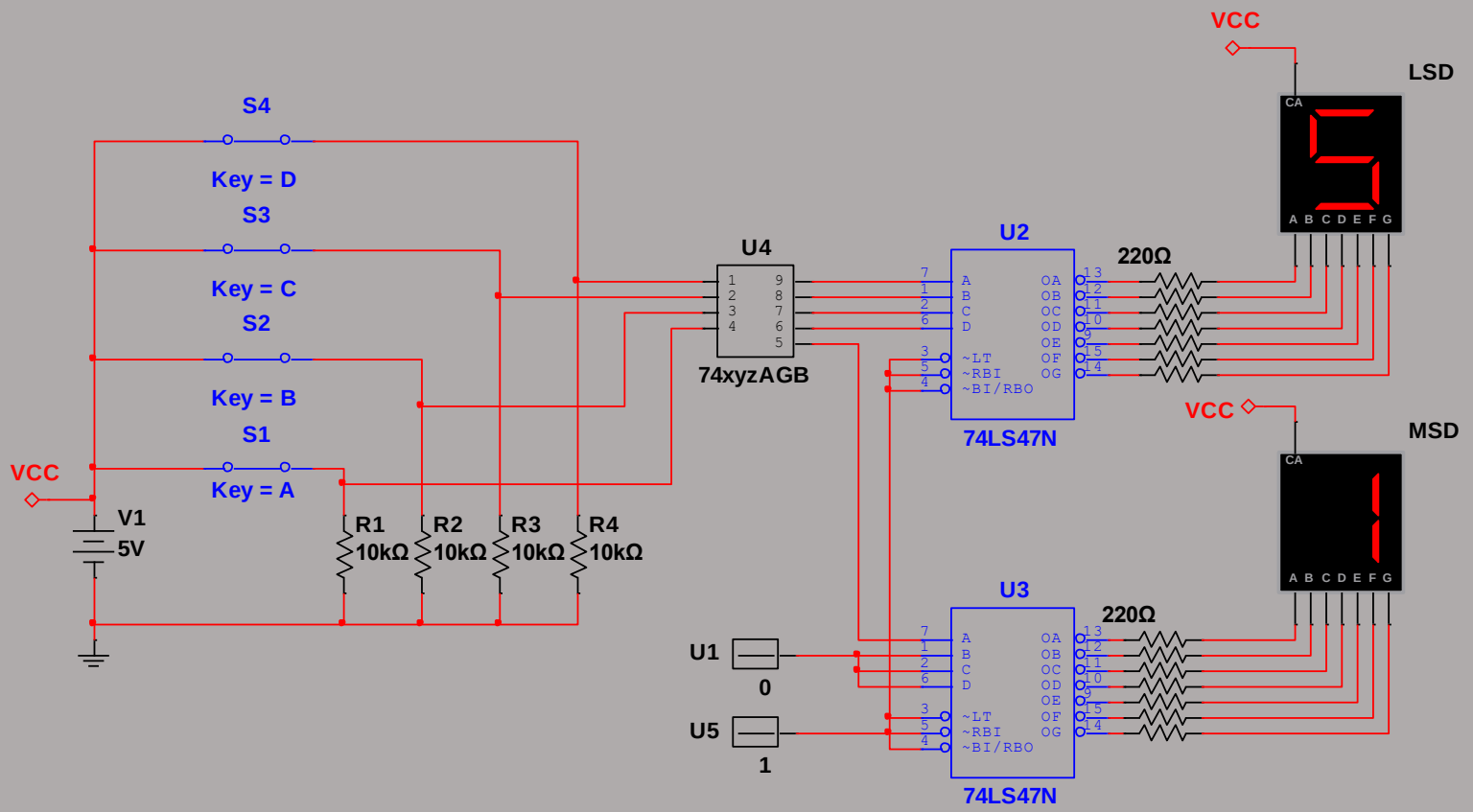
Observations for labs 1-10

- Initially we used lab 1 as our build your own lab, and it helped us understand why we were building simulations for lab1-10. lab 9 my B line was flat but it sould of been about 2x larger than A.
- how adders and subtractors work logic wise.
- It also helped with understanding why we are building the mini lou Project.

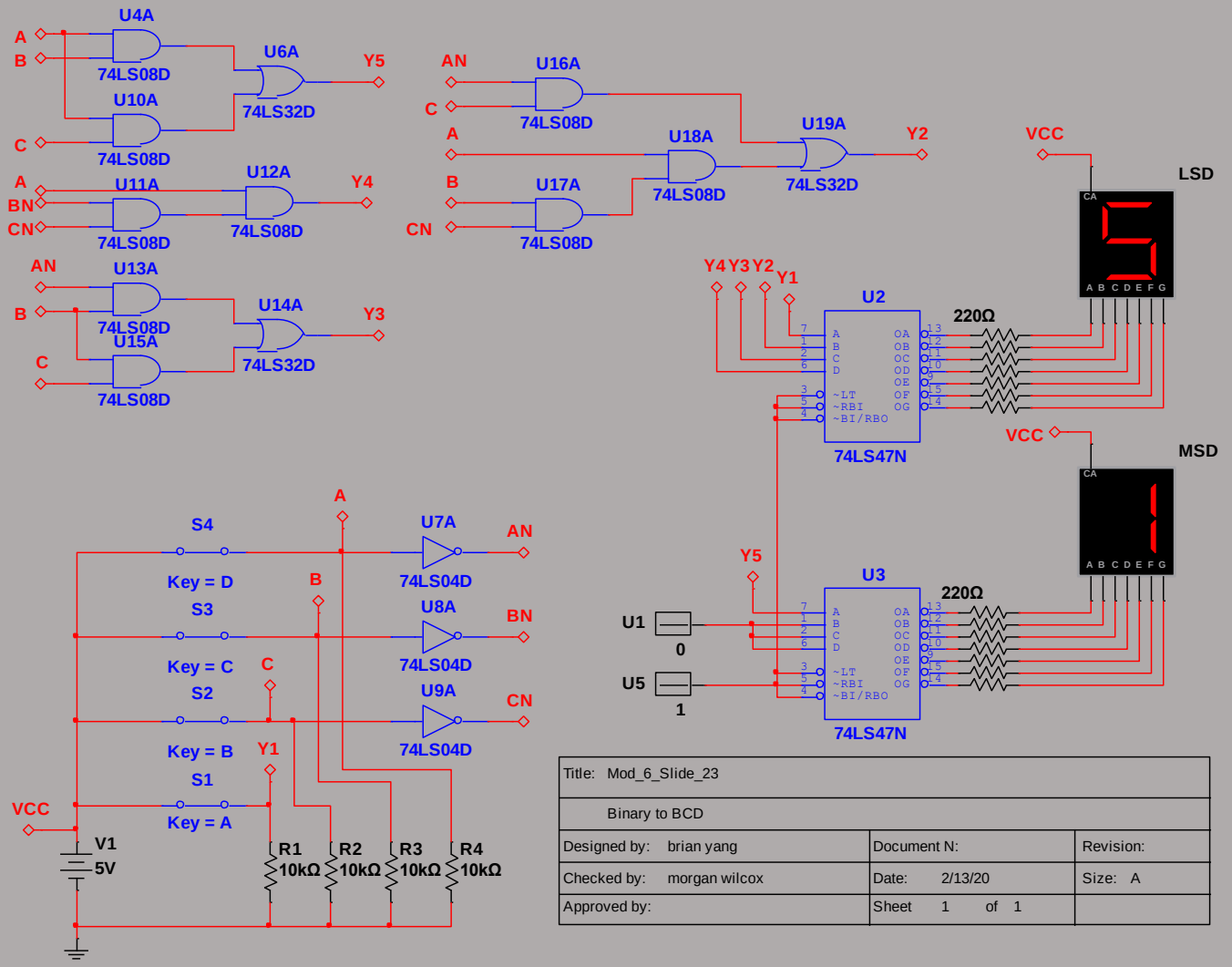
Binary to Bcd Design

- Objective is to design a binary to bcd circuit based on powerpoint slides in module 6

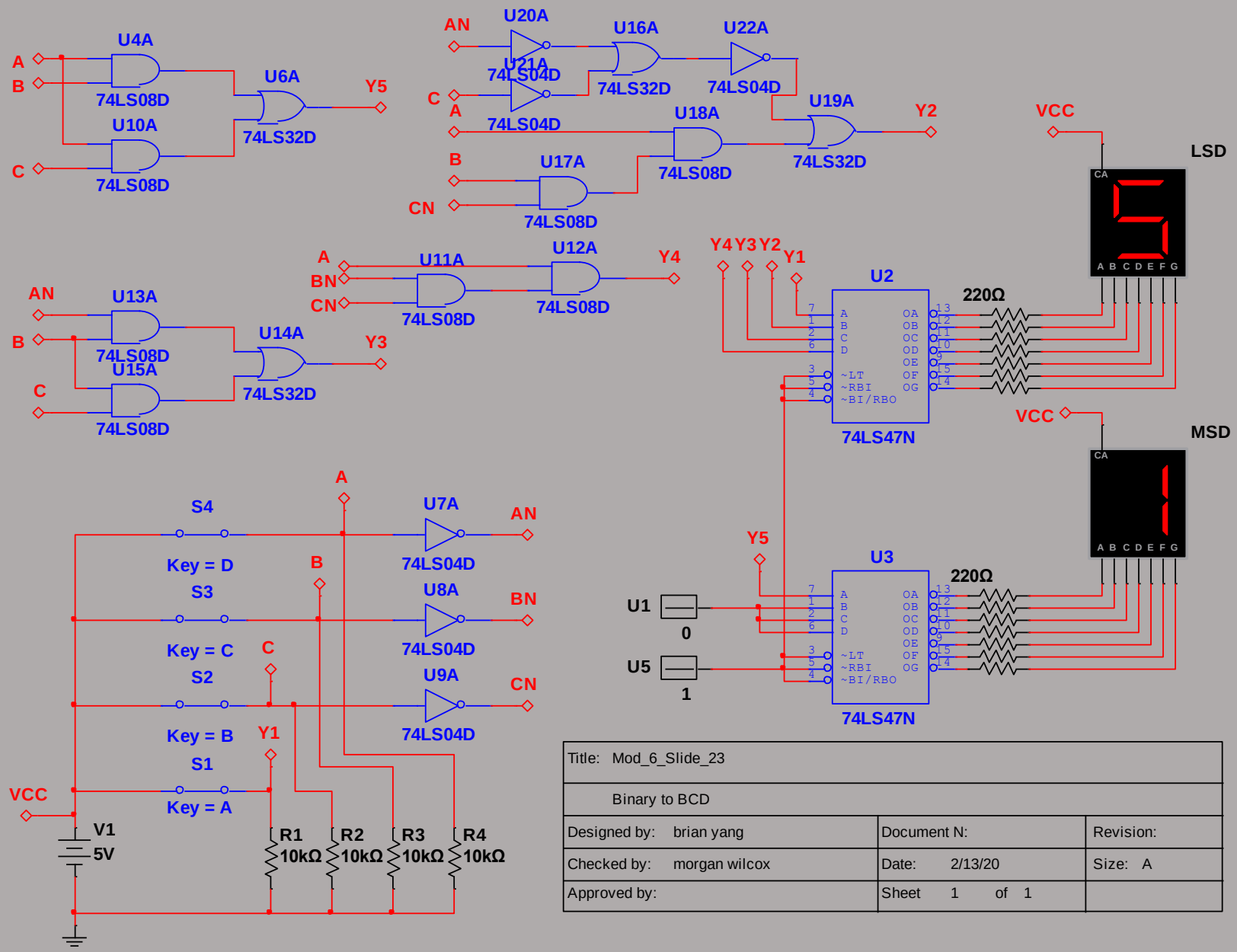
Binary to bcd design slide 23



Binary to bcd slide 25



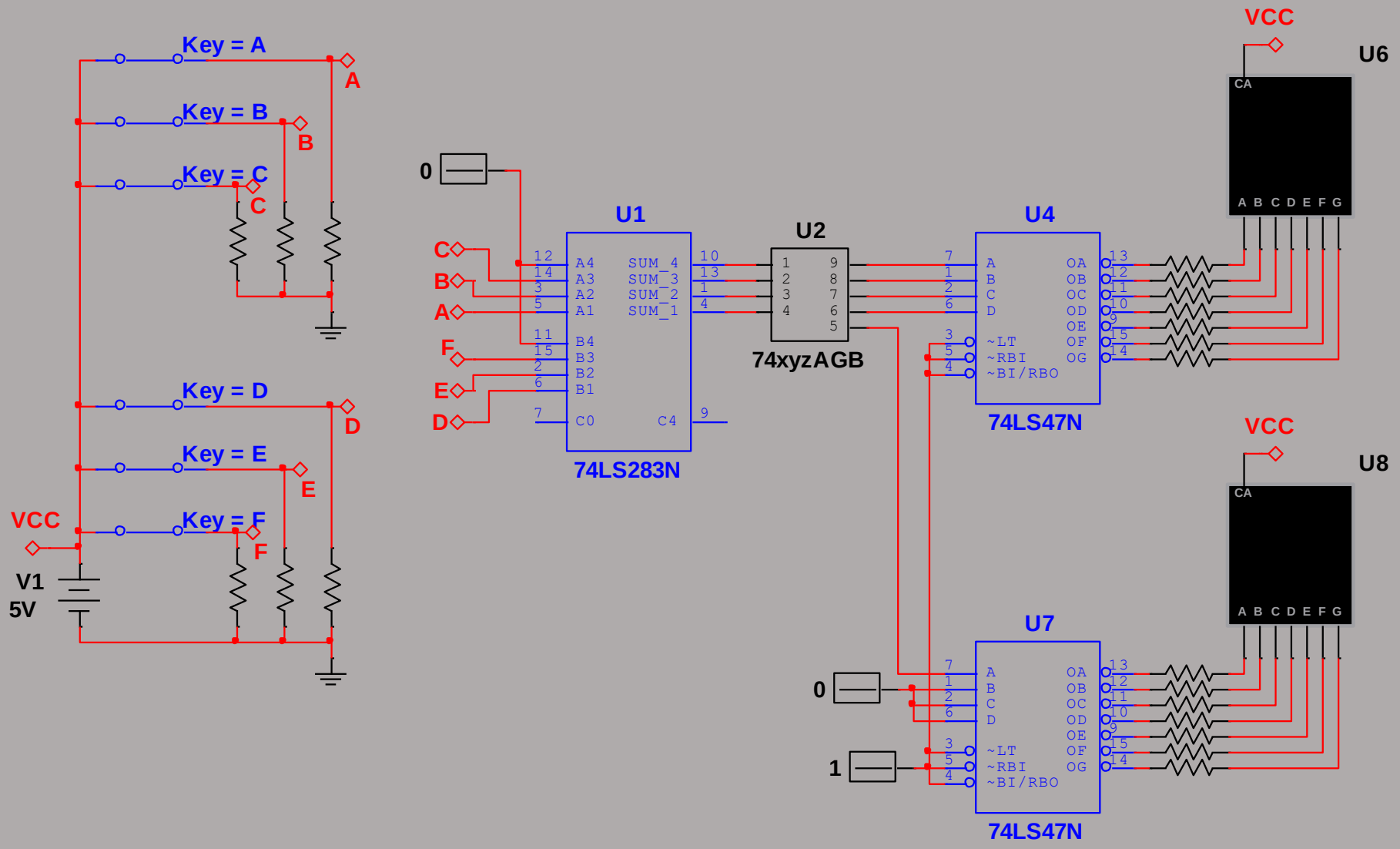
Binary to BCD slide 25 modified



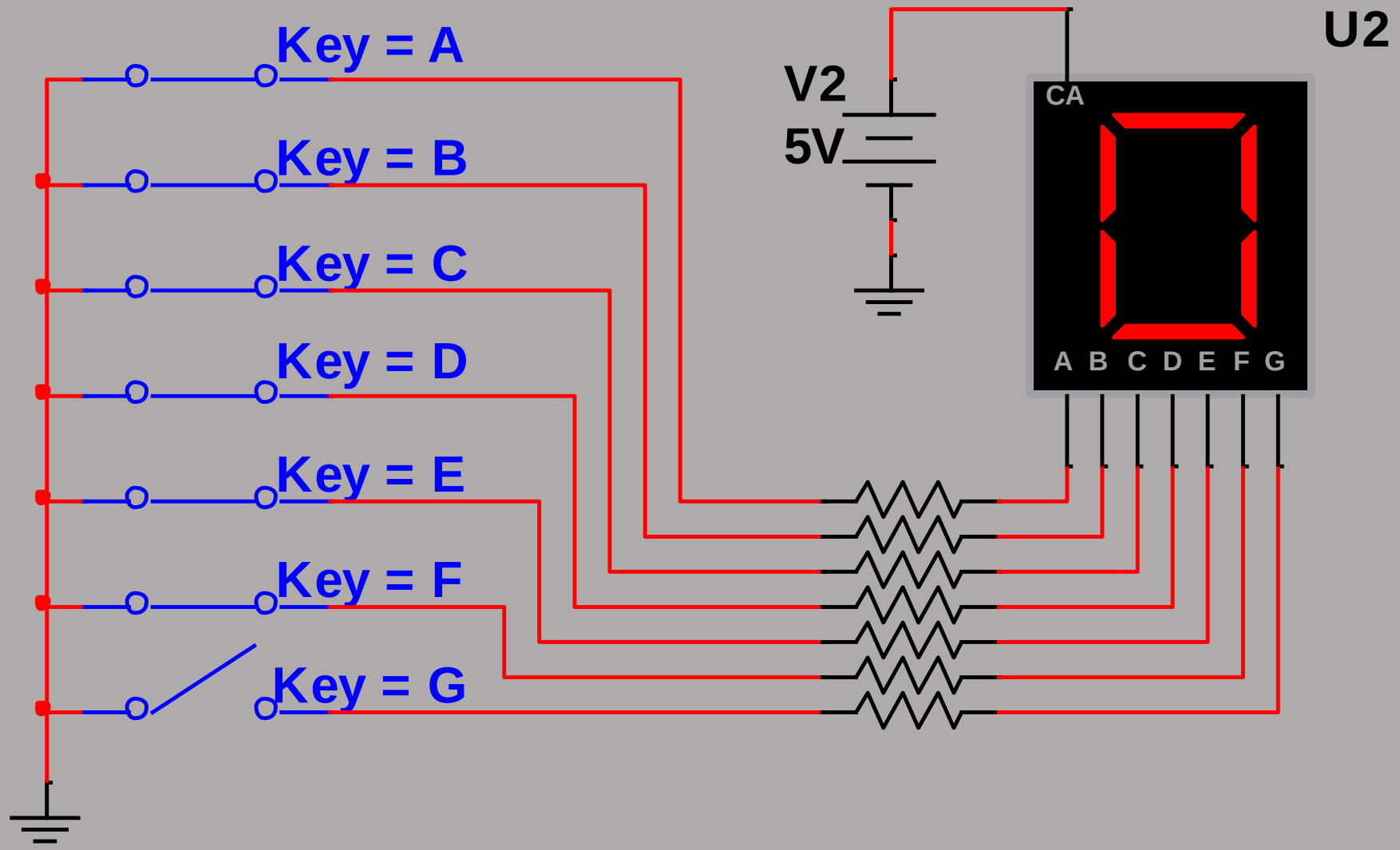
Mini lou part 1

- 3_bit_adder_with_display.ms14 (slide 9) page 37
- seven_segment_common_anode_design.ms14 (slide 11) page 38
- seven_segment_common_cathode_design.ms14 (slide 12) page 39
- common_anode_design.ms14 (slide 13) page 40
- common_cathode_design.ms14 (slide 14) page 41

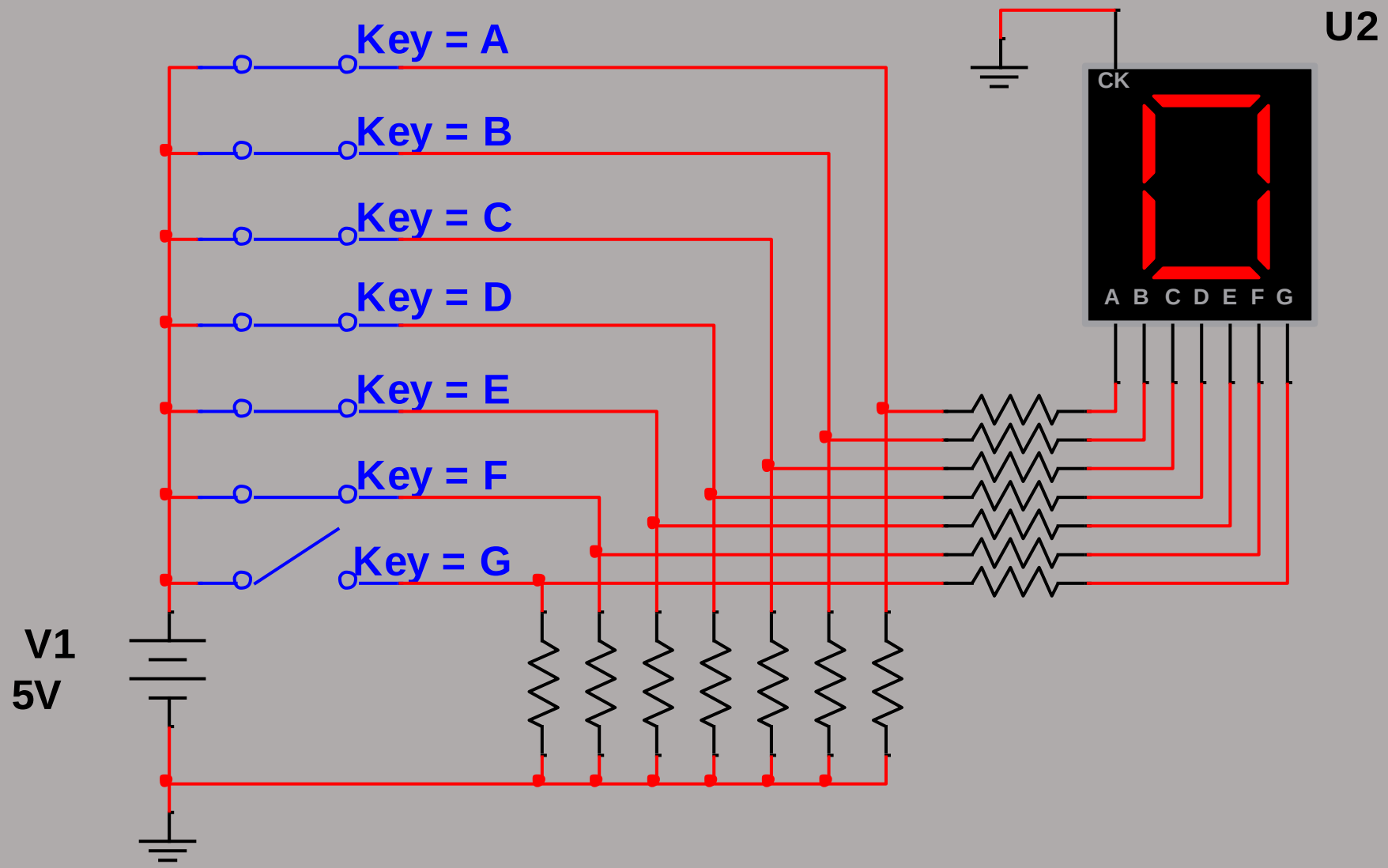
3 bit adder with display.ms14 (slide 9)



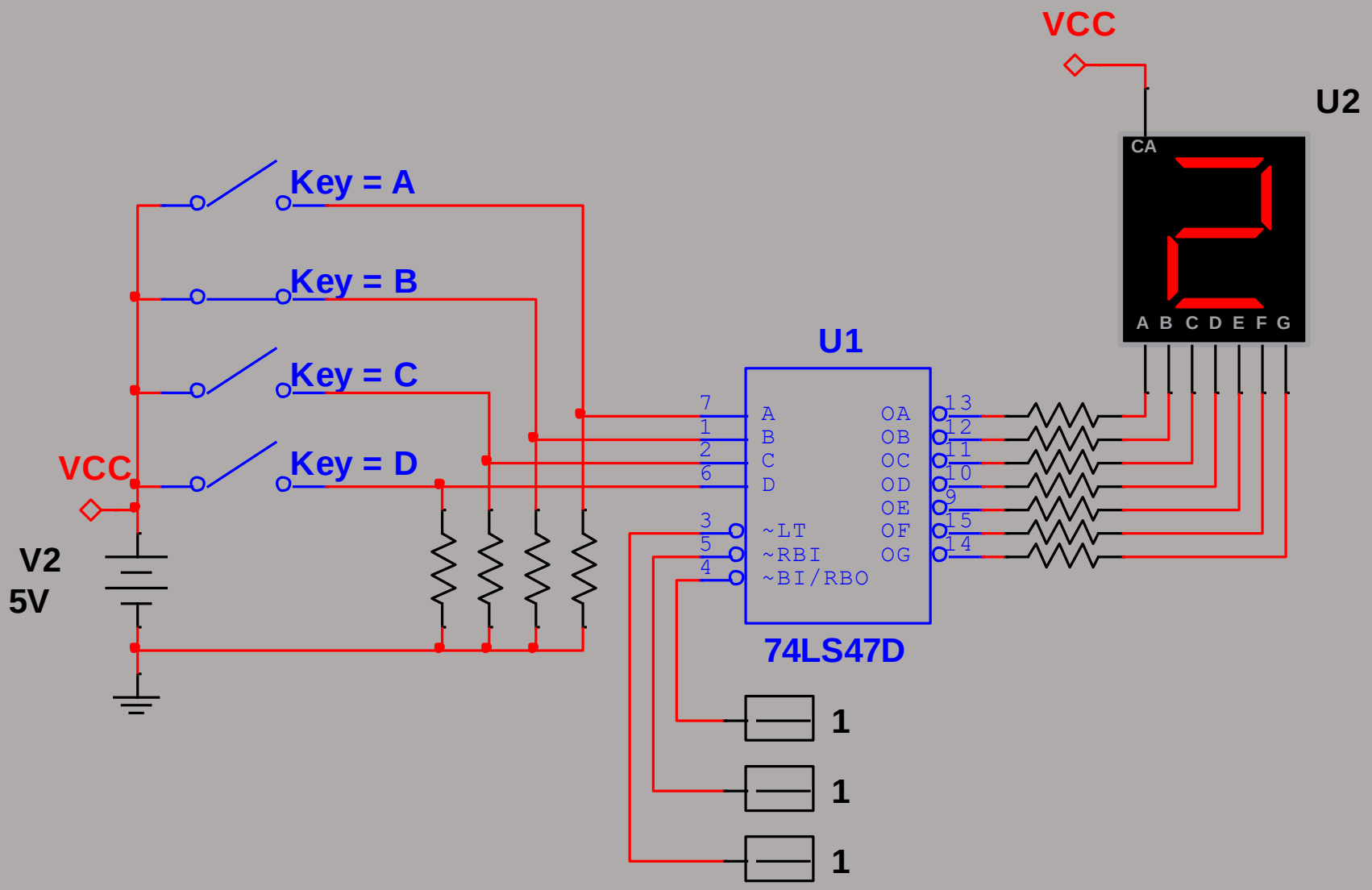
seven segment common anode design.ms14



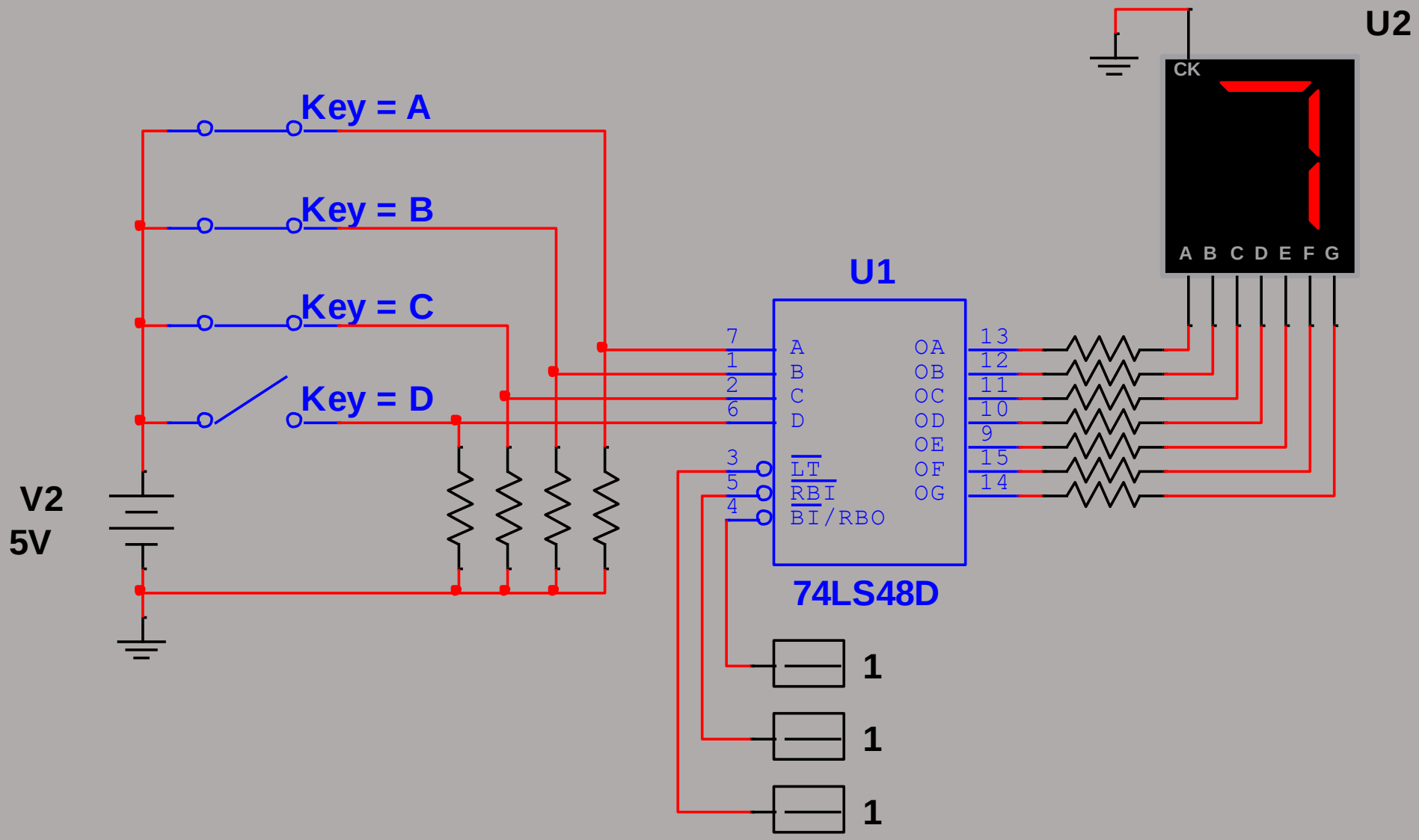
seven segment common cathode design.ms14



common_anode_design.ms14 (slide 13)



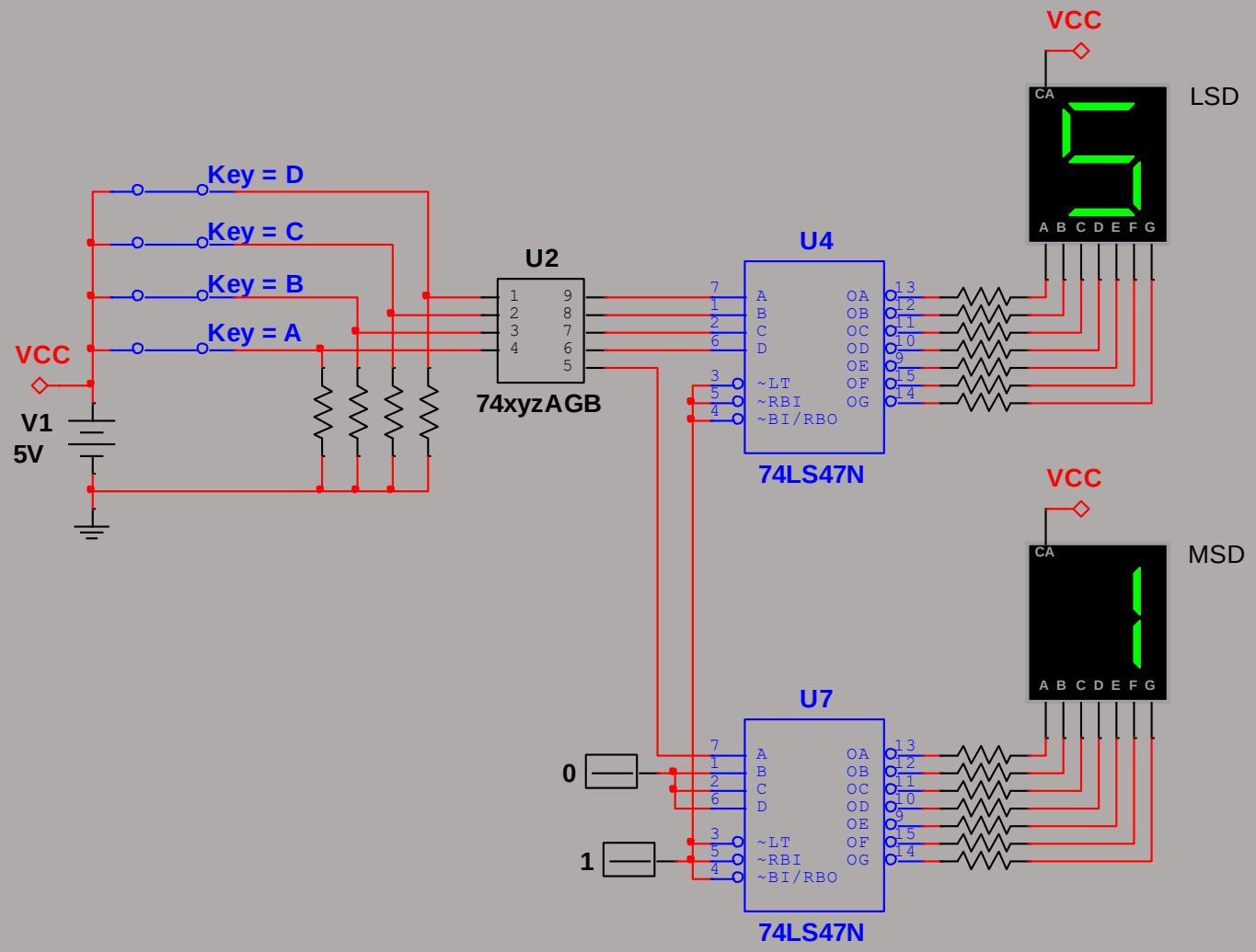
common_cathode_design.ms14 (slide 14)



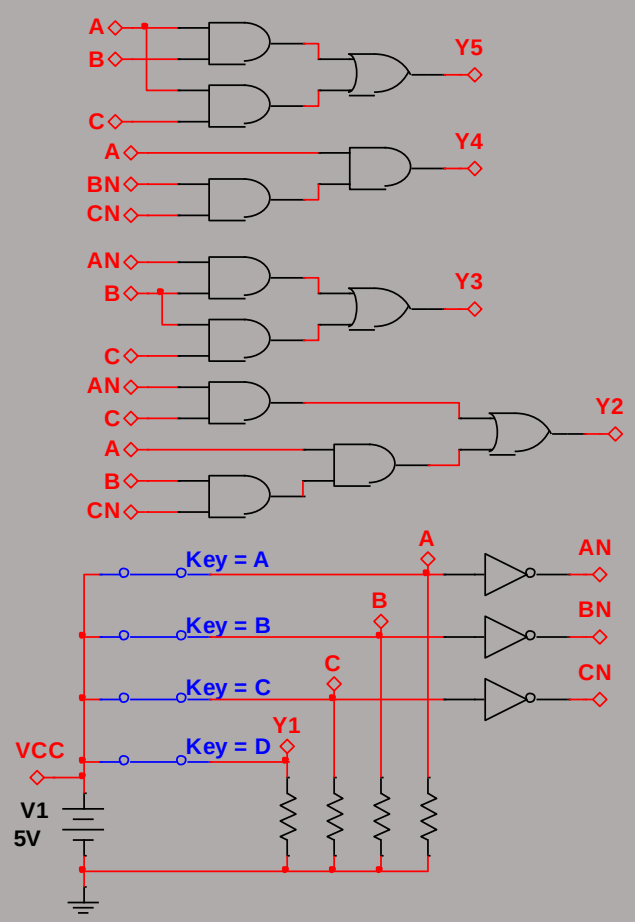
Mini-Lou Part 2 .

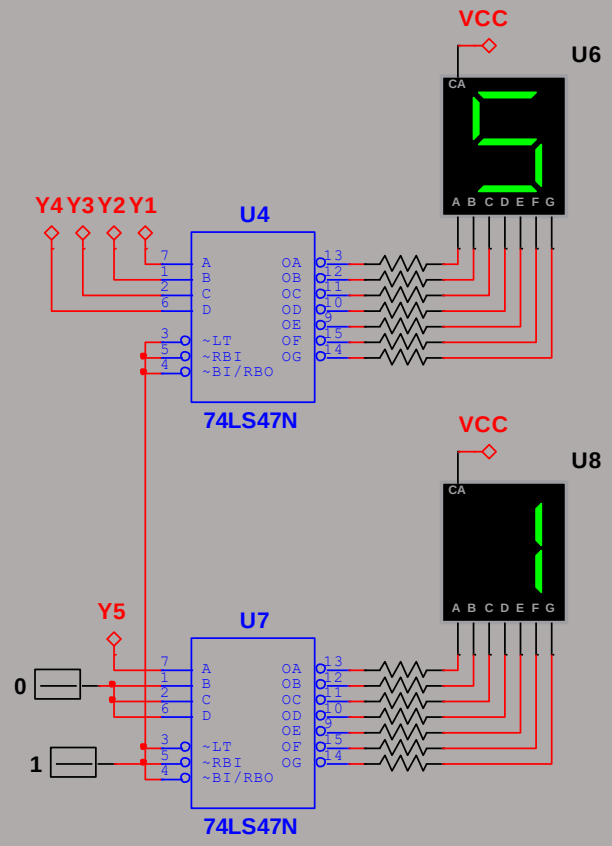
When Lou originally designed the project he used some 74185 Binary-to-BCD converters and now these parts are obsolete. You will need to redesign this function in Multisim and build a circuit using other parts which perform the same function. This is Option 1 on slide 26. OBTW, the design goal is to use the fewest parts possible.

74xyzABC test.ms14



74xyzABC test 2.ms14

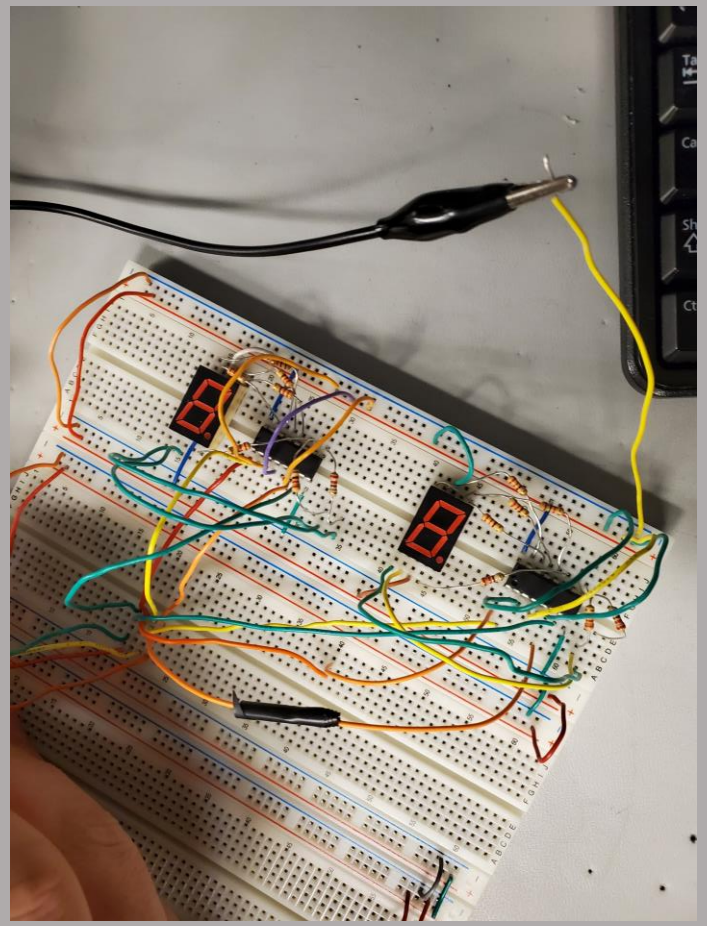


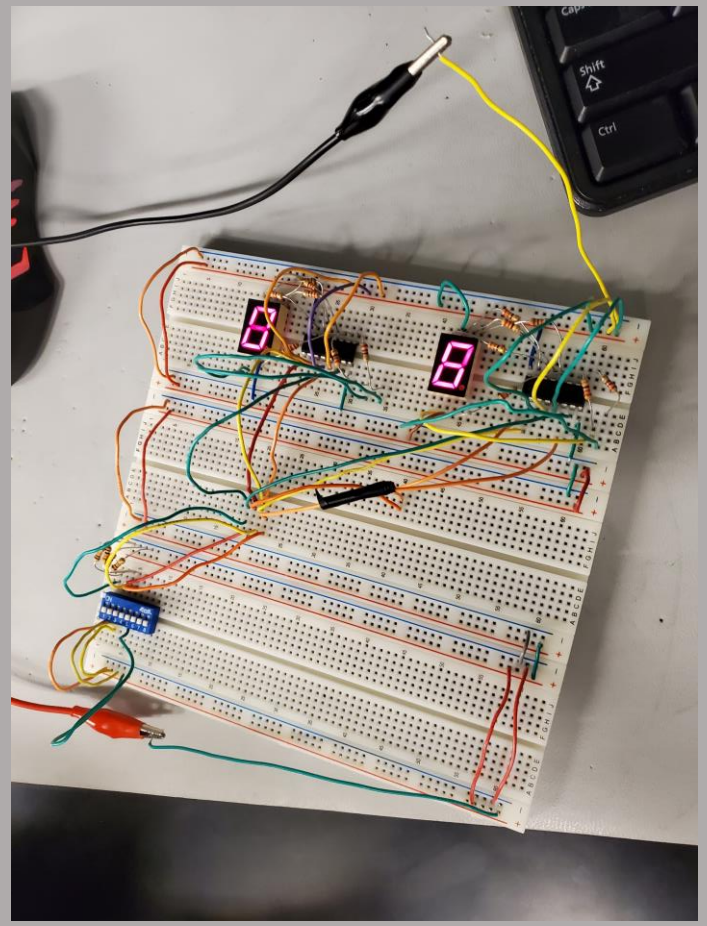


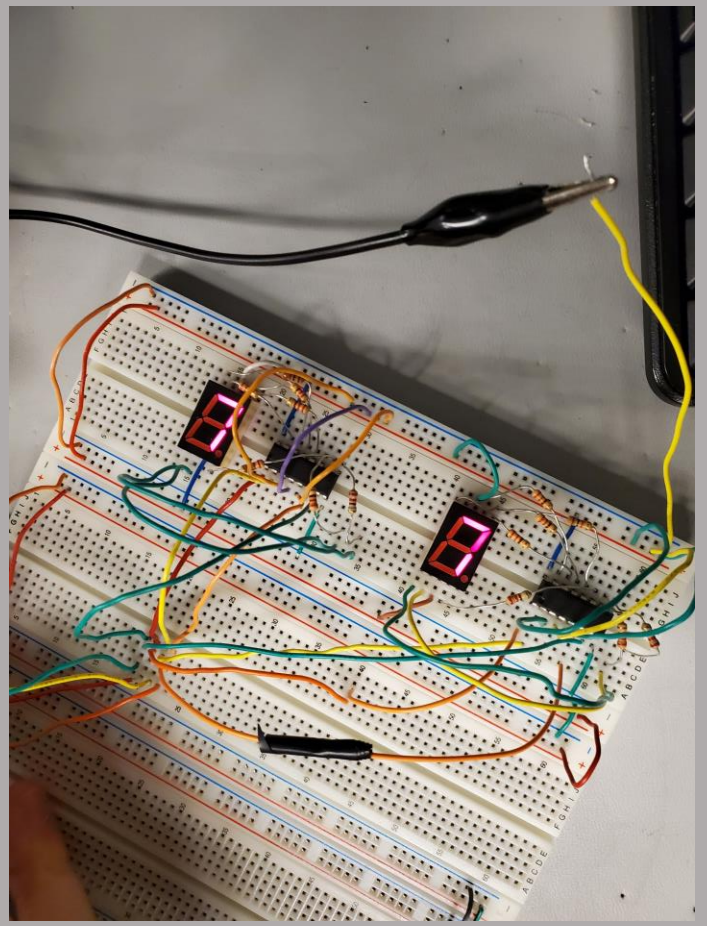
Mini lou part 3

- Section 1 - Design, Build and Test a two digit 7 segment display
- Section 2 - Design, Build and Test the front end that adds or subtracts two 3 bit words.
- Section 3 - Design, Build and Test a 4 bit binary value into BCD to support values from 00 to 15. This section must be designed by you using combinational logic (AND, OR, NAND, NOR etc.)

Section 1 - Design, Build and Test a two digit 7 segment display



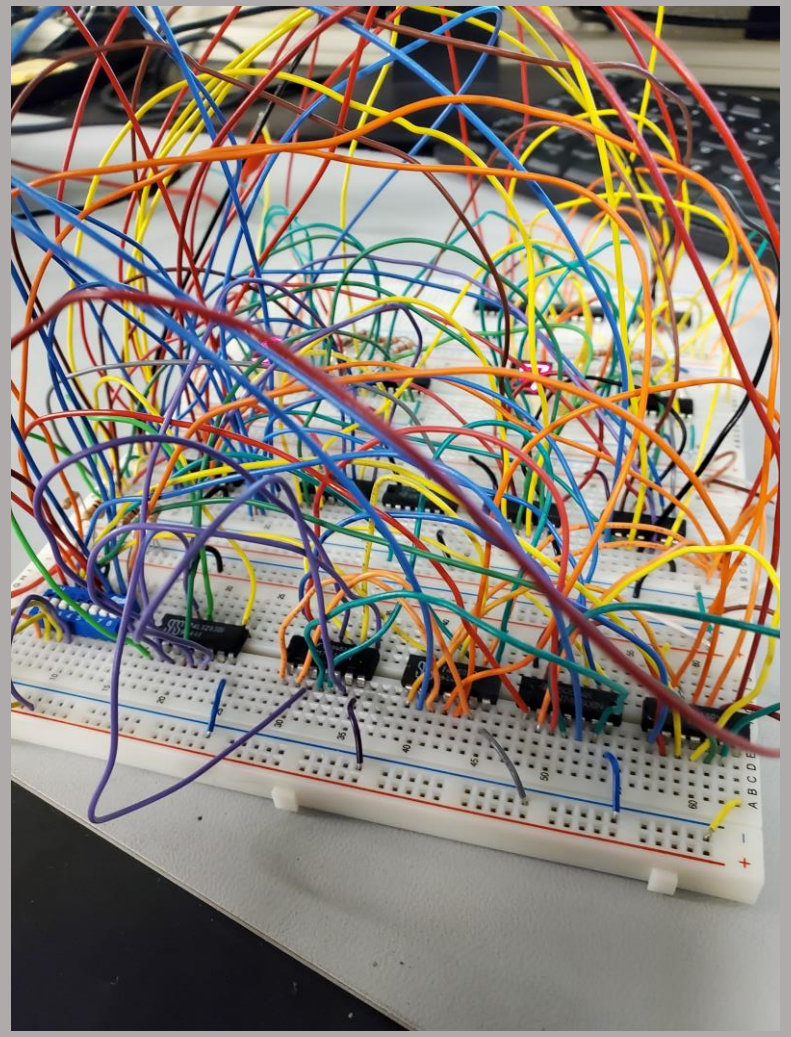


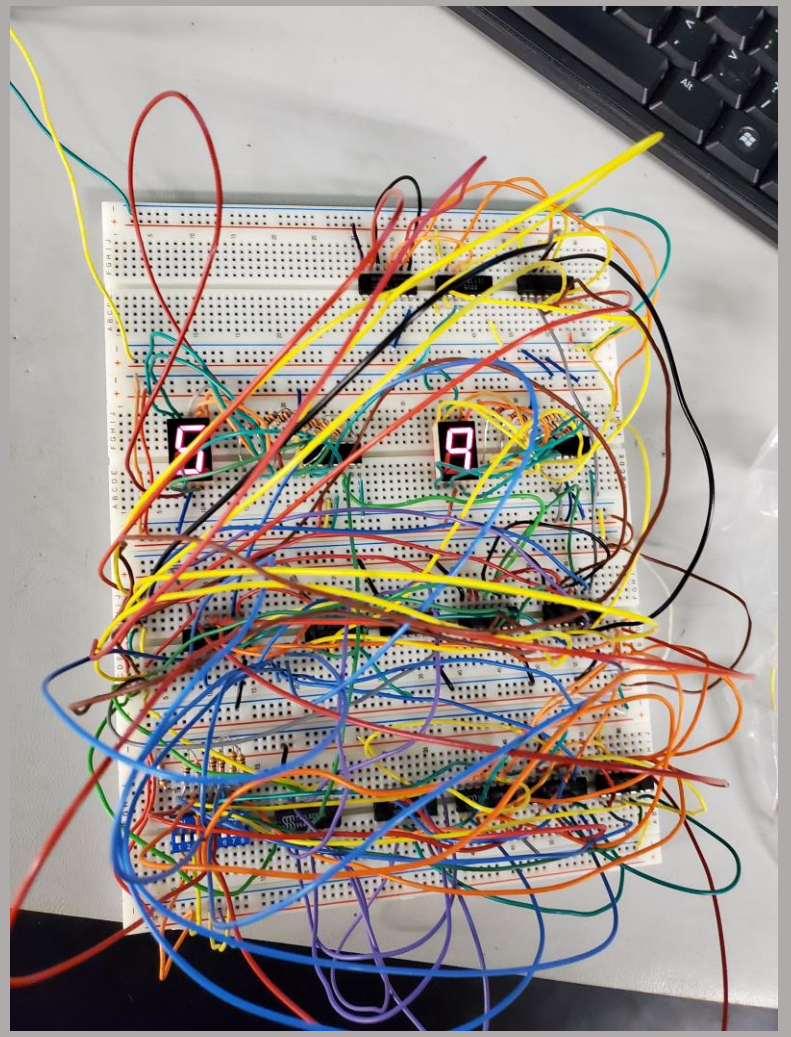


Section 1 observations

This was a very straight forward build after we made sure to check data sheets. Initially we looked at a cathode design data sheet but was using an anode 7 segment display. Both displays functioned properly and outputted the proper numbers after we confirmed the correct data sheet.

Section 2 - Design, Build and Test the front end that adds or subtracts two 3 bit words.

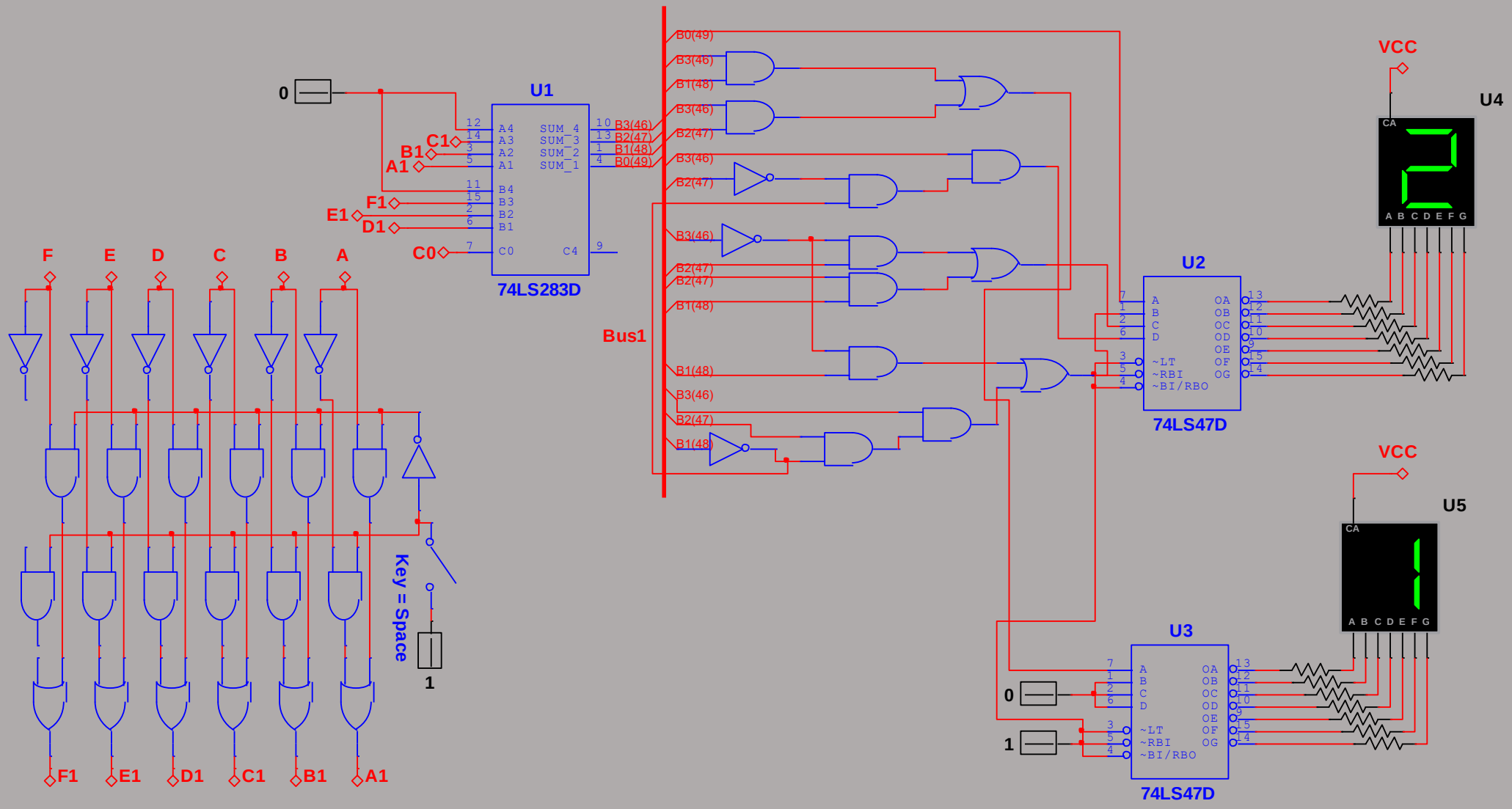




Section 2 observations

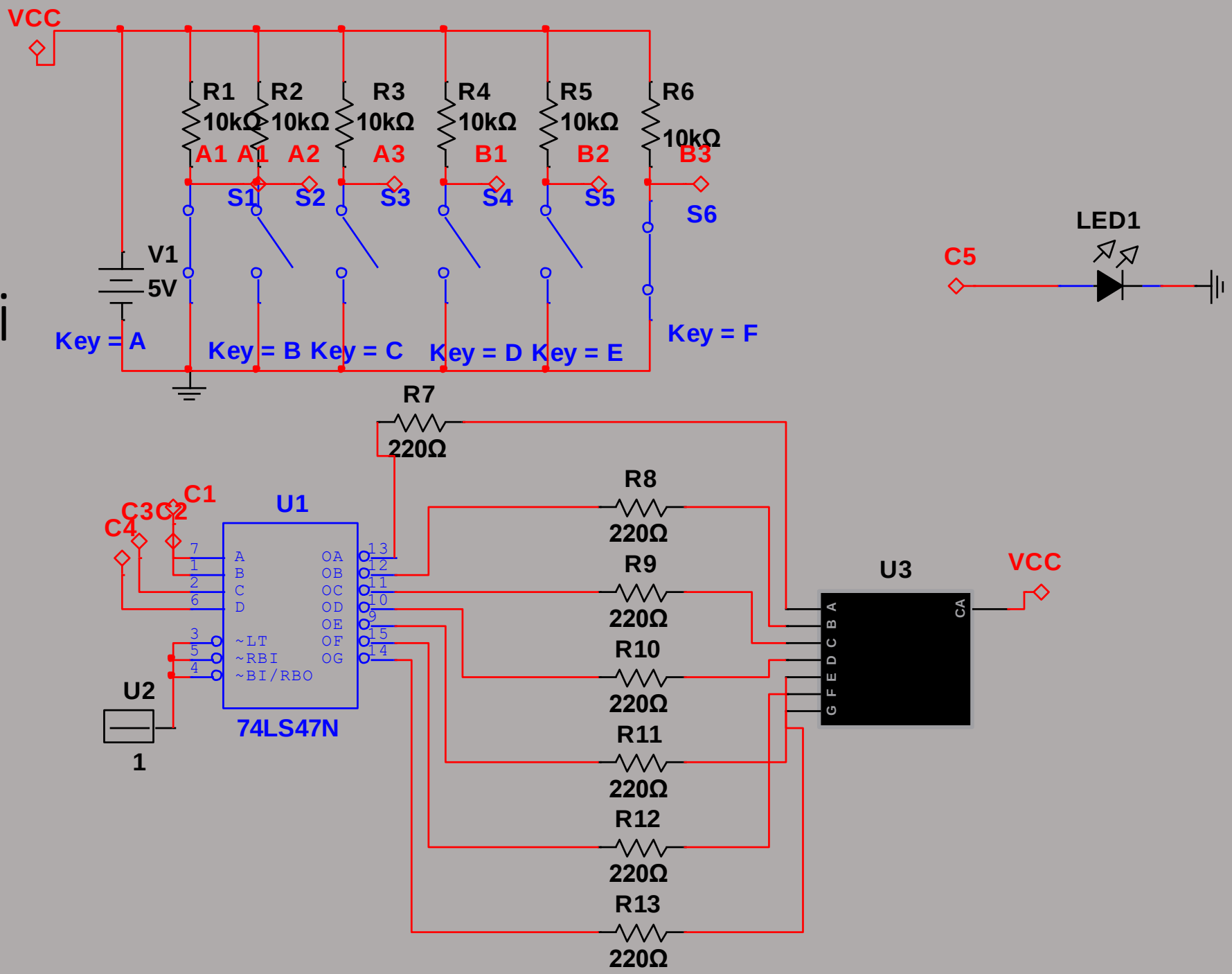
- We did not cut any wires for this portion because it was a test to see if our +/- worked properly also was the thinner copper wire we found out of a box as there was not much wire available at the time of this lab.
- we couldn’t figure out where we had A short happening we had an excess of parts per Mr. Bell saying the goal was the fewest parts possible.
- Our next approach would have been to look back at the logic and figure out where we messed up our equation so we would have had to use an extra chip

Section 3 mini lou design



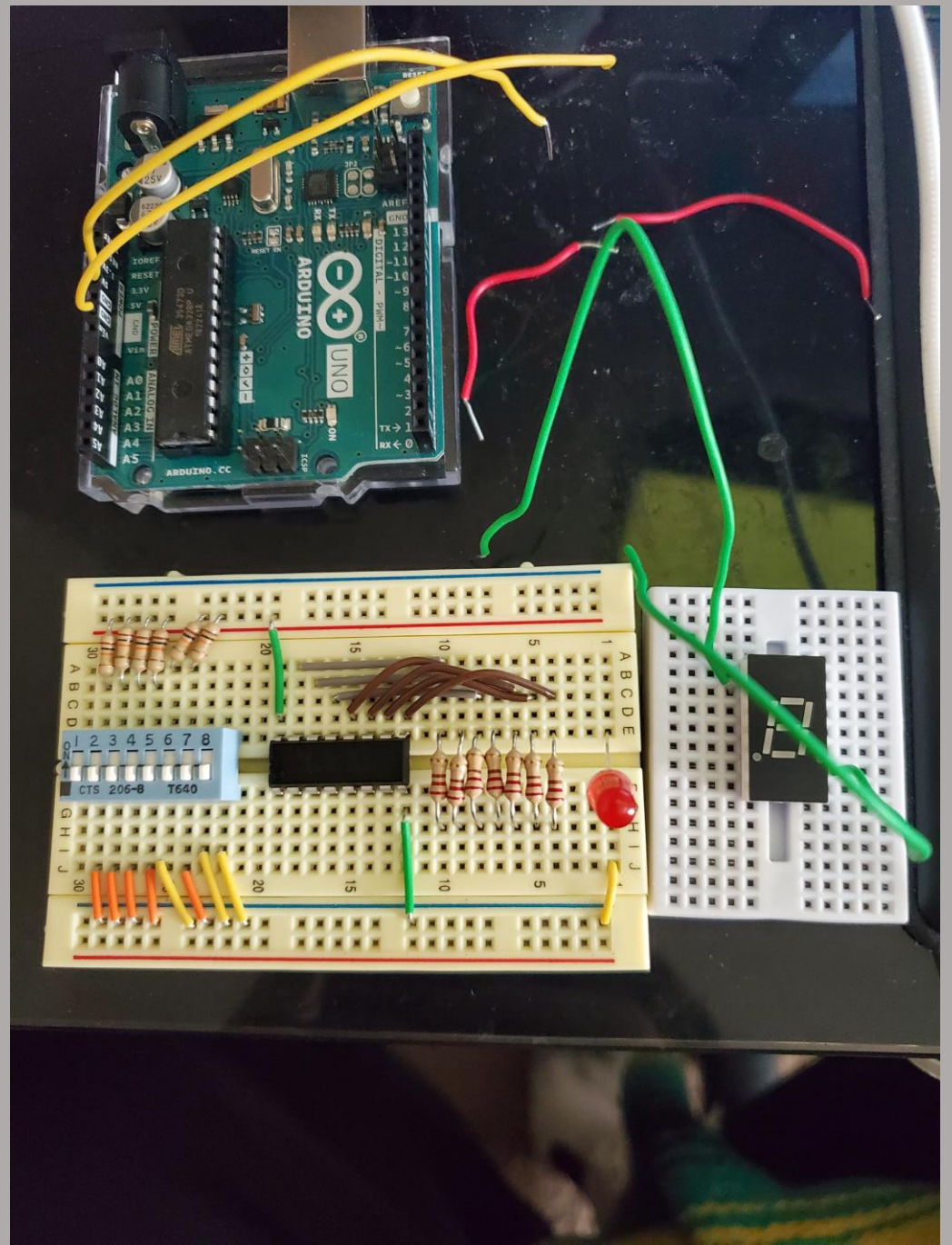
Arduino mini lou

Arduino mini lou version sim

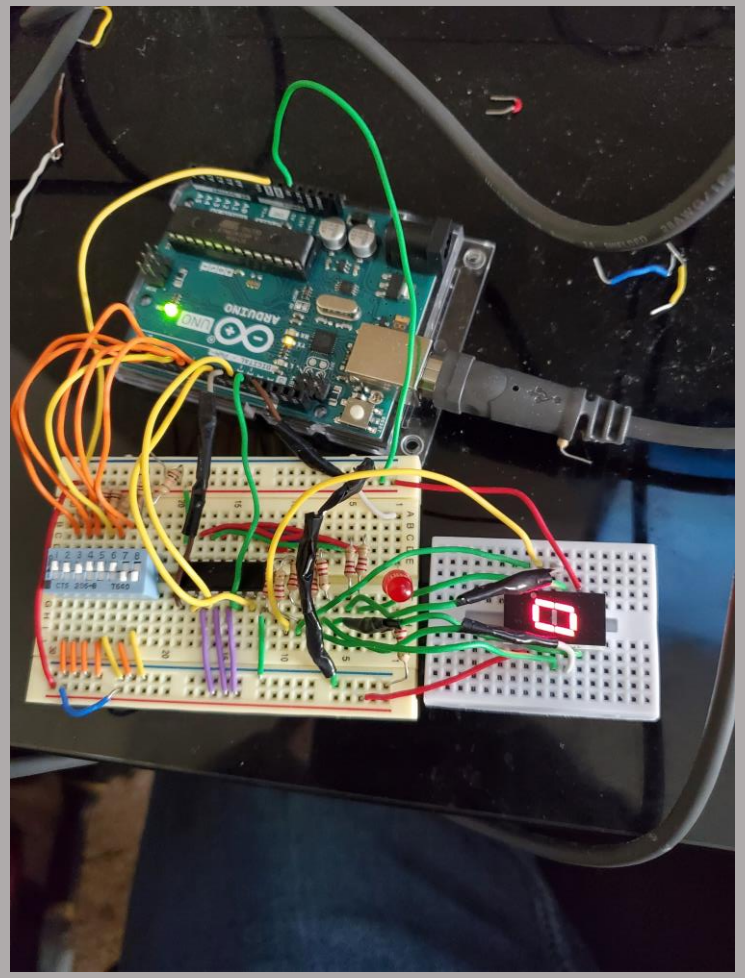


Arduino lou

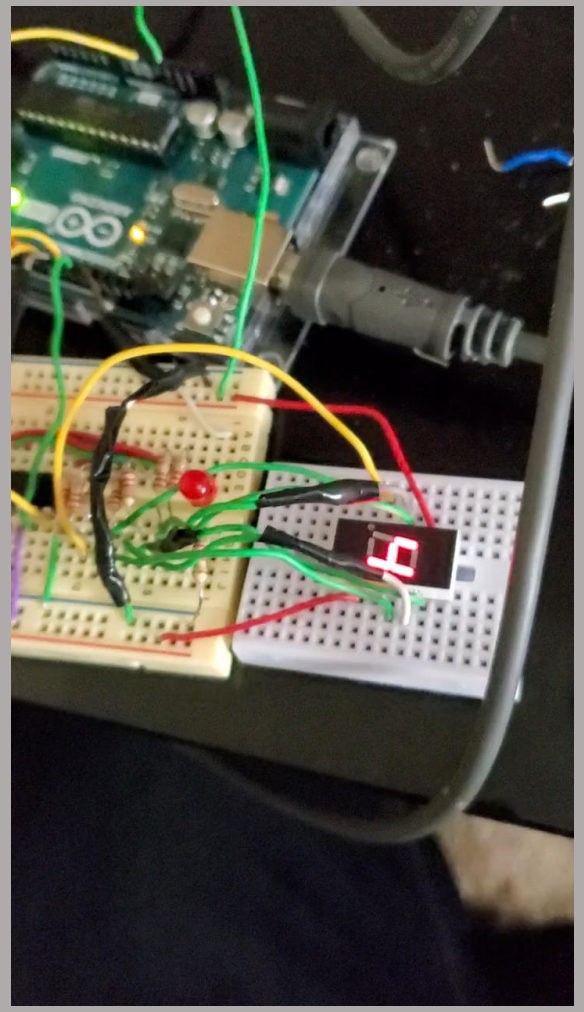
Build before revision



Arduino Mini lou



Video



Click Play ->

Arduino mini lou observations

- I could not get the display to output properly because it was outputting values with missing segments and thought it was the 74ls47n chip since I had bent one of the legs pretty bad redesigning my breadboard. I rechecked the data sheet but it was correct. I then checked the code and that seemed to be correct next step for me was to unhook everything and rewire it again. I Still had the issue until I looked at the board again about 2 days later while working with miles with his lou, and found my error (only half of the board was being supplied ground). I wired up ground to the other side of the board and everything functioned 100%

EECT 122

- Thank you for teaching a great class Mr.Bell!