EECT 112

LAB NOTEBOOK, FALL 2019

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3 LAB 1

- The purpose of lab 1 was to learn how to create logic levels for digital circuits using switches and resistors.
- Using a dip switch, four resistors, and a digital multimeter, create high and low digital signals.
- Use mulitsim to build and simulate the provided electrical diagrams

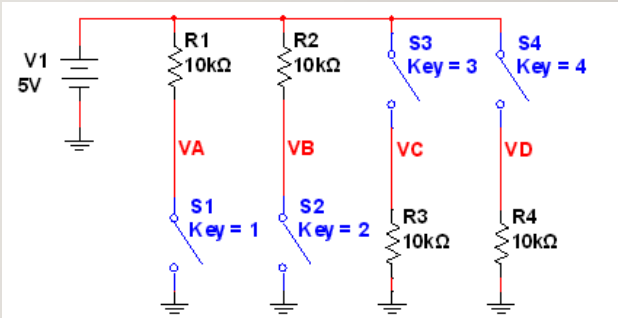
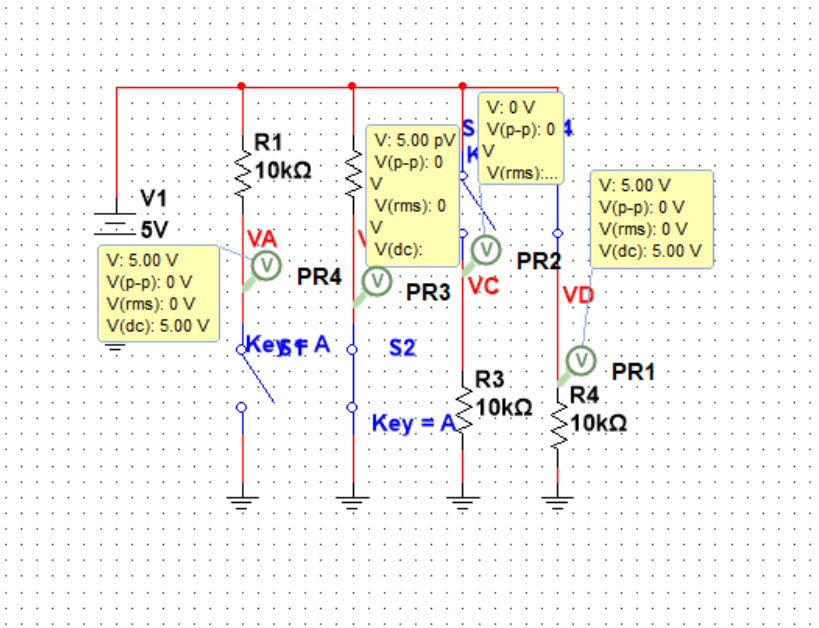


Figure 1- Lab 1 Schematic

LAB 1

- Voltages for the circuits were recorded in multisim and then built in the lab and measured in real life. All voltages were recorded.



Simulated			
S3	S4	VC	VD
open	open	500uV	500uV
open	closed	500uV	5V
closed	open	5V	500uV
closed	closed	5V	5V

Test			
S3	S4	VC	VD
open	open	0	0
open	closed	0	5
closed	open	5	0
closed	closed	5	5

Table 2 (Simulation vs Test)

Simulated			
S1	S2	VA	VB
open	open	5V	5V
open	closed	5V	50nV
closed	open	50nV	5V
closed	closed	50nV	50nV

Test			
S1	S2	VA	VB
open	open	5.01	5.019
open	closed	5.019	0
closed	open	0	5.019
closed	closed	0	0

Table 1 (Simulation vs Test)

5 LAB 1 OBSERVATIONS

- The difference in voltages were not behaving as I originally expected, which was an interesting learning experience.
- The real life lab experiments just showed zero volts instead of 500uV in the multisim. The lab equipment might not be Advanced enough to show readings that low

6 LAB 2

- The purpose of lab 2 was to practice converting numbers from one base to another.
- I used the lecture 2 PowerPoint and excels as a reference in the number conversions
- This Lab was just converting numbers using excel, no builds or sim.

7 LAB 2

5 Bit Binary Min	00000	Decimal value =	0
5 Bit Binary Max	11111	Decimal value =	31
8 Bin Binary Max	00000000	Decimal value =	0
8 Bin Binary Min	11111111	Decimal value =	255

Lecture 2a Slide 5.xlxs

6 Bit Binary Max	111111	Decimal value =	63
7 Bit Binary Max	1111111	Decimal value =	127

Lecture 2a Slide 7.xlxs

Min Decimal No	0	Binary value =	0
Max Decimal No	63	Binary value =	111111

Lecture 2a Slide 9.xlxs

Min Decimal No	0	Binary value =	0000
Max Decimal No	15	Binary value =	1111

Lecture 2a Slide 12.xlxs

Min Hexadecimal No	0	Decimal value =	0
Max Hexadecimal No	FFF	Decimal value =	4095

Lecture 2a Slide 14.xlxs

Hexadecimal	Decimal
000	0
03F	63
07F	127
0FF	255
FFF	4095

Lecture 2a Slide 18.xlxs

Max Decimal value =	450
Hexadecimal value =	1C2
Binary value =	111000010

LAB 3

- Lab 3 was about learning how AND/OR gates work and how to measure their outputs.
- Multisims of the provided circuit diagrams were made and simulated to get simulated data. Then, breadboards were constructed in the lab and real life data was taken.
- Equipment needed:

1 – Digital Multimeter

2 – 10Kohm

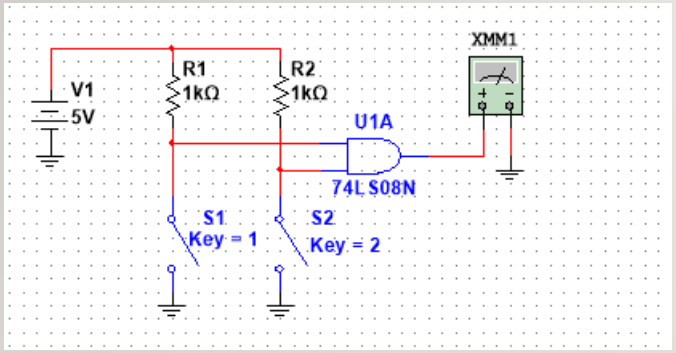
1 – 4 position dip switch

1 – 74LS08

1 – 74LS32

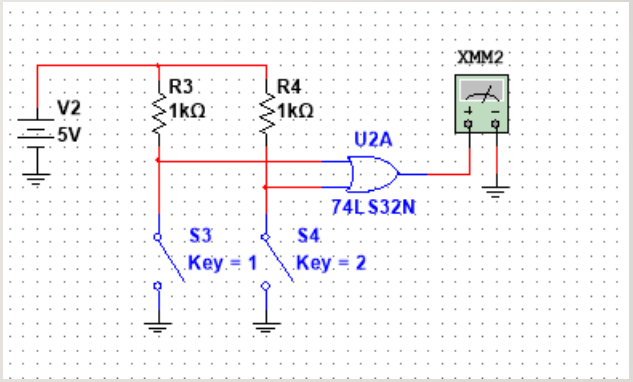
9 LAB 3

AND gate circuit



		Simulated	Test
S1	S2	Output	Output
Open	Open	5v	4V
Open	Closed	0v	0.3V
Closed	Open	0v	0.3V
Closed	Closed	0v	0.3V

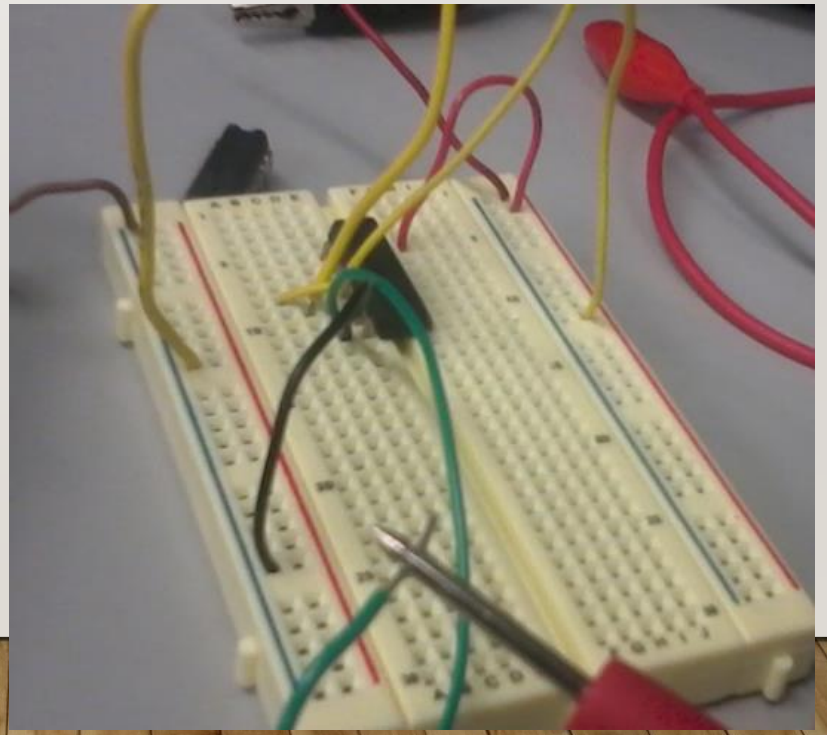
OR gate circuit



		Simulated	Test
S1	S2	Output	Output
Open	Open	5v	4.05V
Open	Closed	5v	4.05V
Closed	Open	5v	4.1V
Closed	Closed	0v	0.4V

10 LAB 3

- Observations: In multisim, the simulated voltages were 5V and 0V. The real life circuit had 4V and and .34V. This may be to ambient electricity in some of the systems.



LAB 4

- The object of lab 4 was to continue learning how to describe Logic Circuits algebraically.
- Multisims of the provided circuit diagrams were made and simulated to get simulated data. Then, breadboards were constructed in the lab and real life data was taken.
- Equipment needed:

1 – Digital Multimeter

3 – 10Kohm

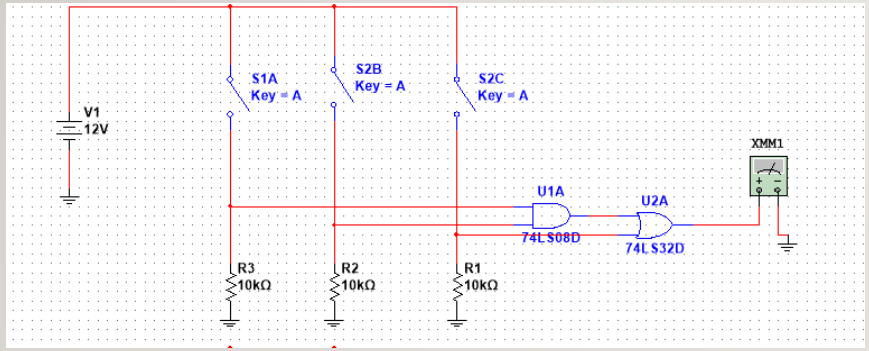
1 – 4 position dip switch

1 – 74LS08

1 – 74LS32

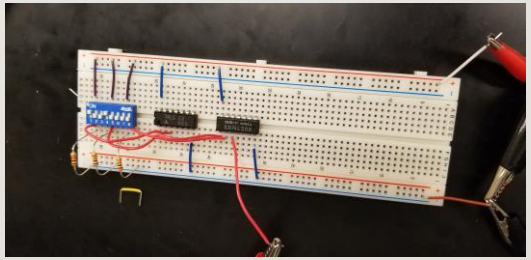
12 LAB 4

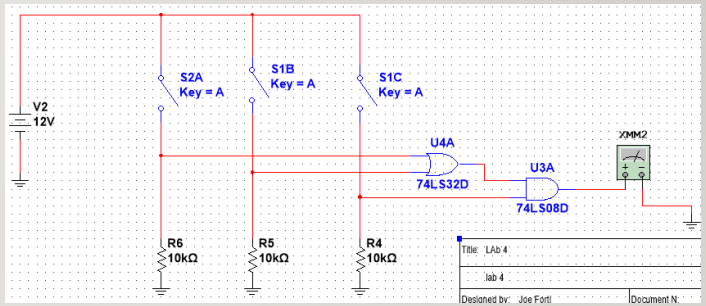
Circuit One



S1	S2	S3	Simulated Output	Test Output
Open	Open	Open	0	.1
Open	Open	Closed	5	4.3
Open	Closed	Open	0	.1
Open	Closed	Closed	5	4.3
Closed	Open	Open	0	.1
Closed	Open	Closed	5	4.3
Closed	Closed	Open	5	4.3
Closed	Closed	Closed	5	4.3

Circuit two





S1	S2	S3	Simulated Output	Test Output
Open	Open	Open	0	0
Open	Open	Closed	0	.1
Open	Closed	Open	0	.1
Open	Closed	Closed	5	4.5
Closed	Open	Open	0	.14
Closed	Open	Closed	5	4.5
Closed	Closed	Open	0	.14
Closed	Closed	Closed	5	4.5

LAB 4

- Observations: 1k Ohms resistors were needed to achieve Proper voltage levels.

14 LAB 5

- Lab 5 was to learn how two input logic gates work using digital ICs, switches and resistors.
- Multisims of the provided circuit diagrams were made and simulated to get simulated data. Then, breadboards were constructed in the lab and real life data was taken
- Equipment needed:

1 – Digital Multimeter

2 – 10Kohm

1 – 4 position dip switch

1 – 74LS04 Hex Inverter

1 – 74LS08 Quad AND

1 – 74LS32 Quad OR

1 – 74LS86 Quad XOR

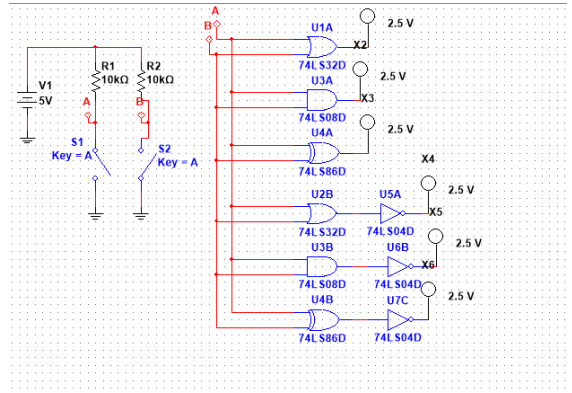
15 LAB 5

This lab was simulation only and these are the results

Simulated

A =	0	0	1	1
B =	0	1	0	1
OR	0	1	1	1
AND	0	0	0	1
XOR	0	1	1	
NOR	1	0	0	0
NAND	1	1	1	0
XNOR	1	0	0	1

Table 1 Simul



16 LAB 7

- The purpose of this lab was to learn how to reduce a circuit design down to the smallest size using the 17 Theorems and Karnaugh maps.
- Multisims of the provided circuit diagrams were made and simulated to get simulated data. Then, breadboards were constructed in the lab and real life data was taken
- Equipment needed:

1 – Digital Multimeter

3 – 10Kohm

1 – 4 position dip switch

1 – 74LS04 Hex Inverter

1 – 74LS00 Quad NAND

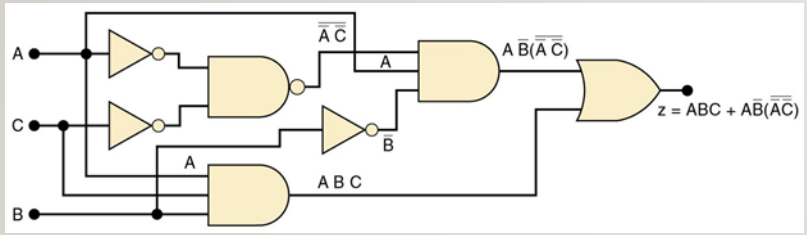
1 – 74LS11 Triple 3 input AND

1 – 74LS32 Quad OR

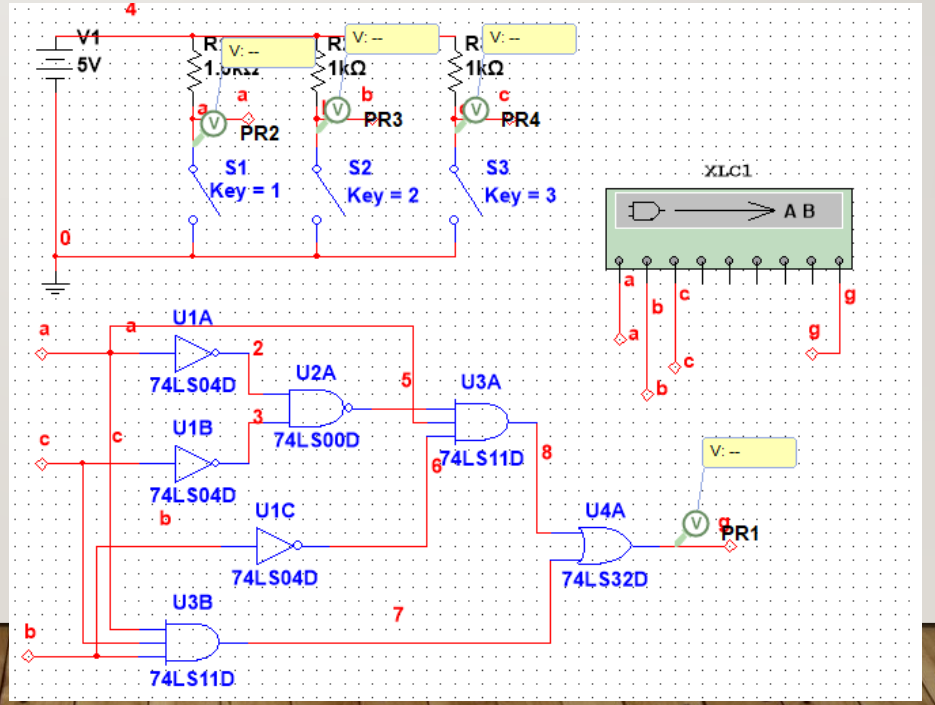
17 LAB 7

One thing that was able to be used in multisim was a logic converter. This was very handy as it allowed rapid procurement of the theorems needed.

Circuit Schematic



Multisim Build



18 LAB 7

- Test and Results: All logic options were test and voltages were recorded. Simulations matched highs and lows, but not actual voltages.

Simulated			
A	B	C	Output
0	0	0	0v
0	0	1	0v
0	1	0	0v
0	1	1	0v
1	0	0	5v
1	0	1	5v
1	1	0	0v
1	1	1	5v

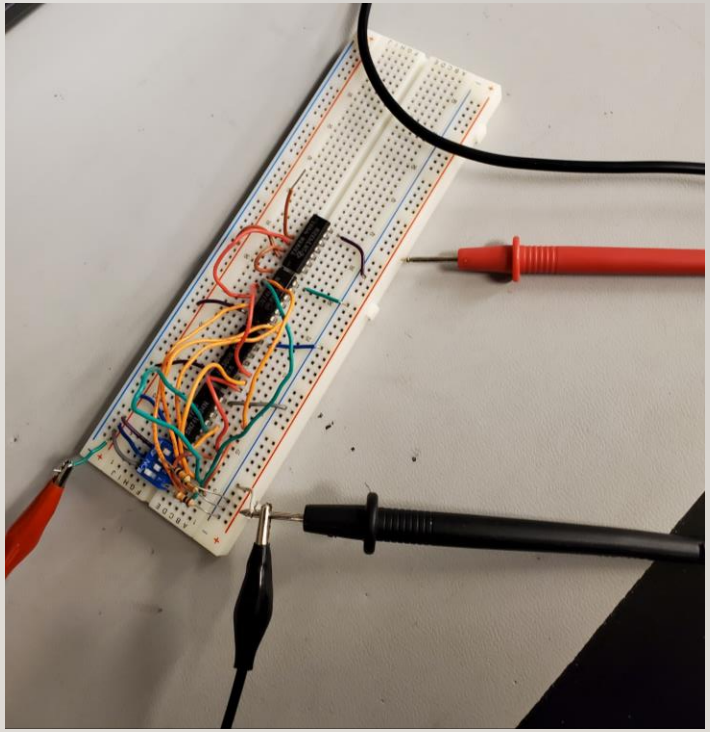
Test			
A	B	C	Output
0	0	0	.1v
0	0	1	.1v
0	1	0	.1v
0	1	1	.1v
1	0	0	3.9v
1	0	1	3.9v
1	1	0	.1v
1	1	1	3.9v

Table 1 Simulation vs Test

A \ BC	00	01	11	10
0	0v	0v	0v	0v
1	5v	5v	5v	0v

X = AB'+AC	SOP form
X =AB'C'+AB'C+ABC	POS form

Table 2 Karnaugh Map of circuit



LAB 7

- Observations:: Voltage didn't get to where it needed to Be with 1k resistors. Make sure resistors are before and after the switch, this can effect the results and make the switch act inverted.

20 LAB 8

- The purpose of Lab 8 was to continue learning how to reduce a circuit design down to the smallest size using the 17 Theorems and Karnaugh maps. The results of lab 7 were needed in the SOP and POS forms, and the goal was to build those two circuits.
- Multisims of the provided circuit diagrams were made and simulated to get simulated data. Then, breadboards were constructed in the lab and real life data was taken
- Equipment needed:

1 – Digital Multimeter

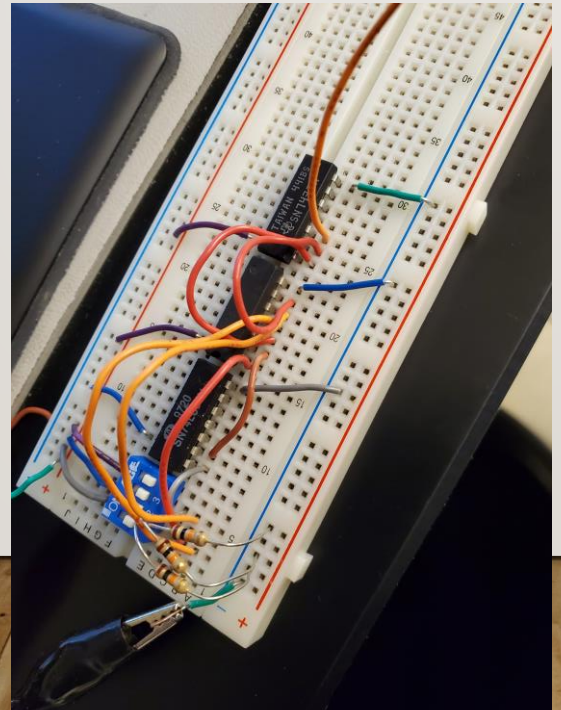
3 – 10Kohm Resitors

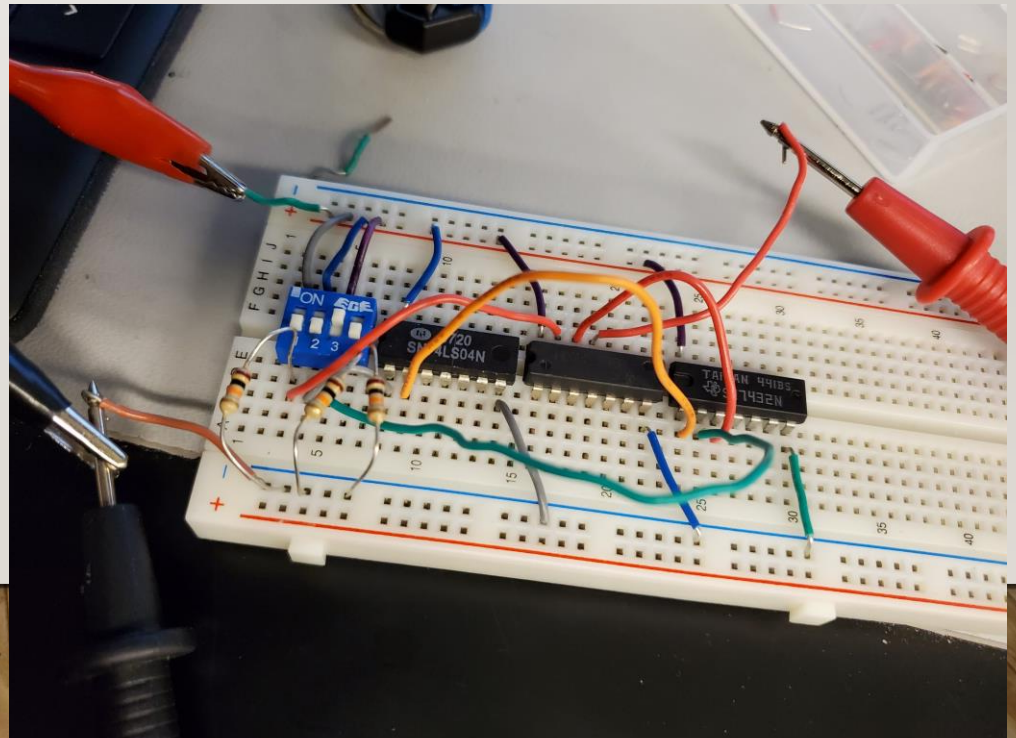
1 – 4 position dip switch

1 – 74LS04 Hex Inverter

1 – 74LS08 Quad AND

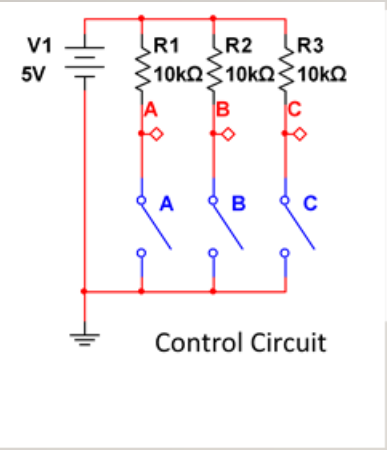
1 – 74LS32 Quad OR

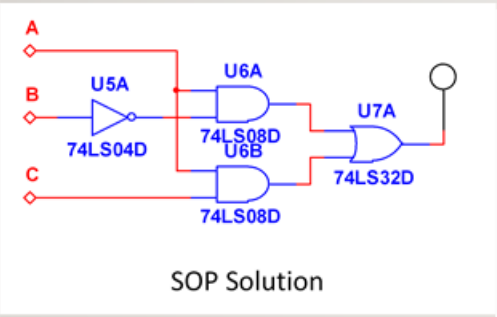


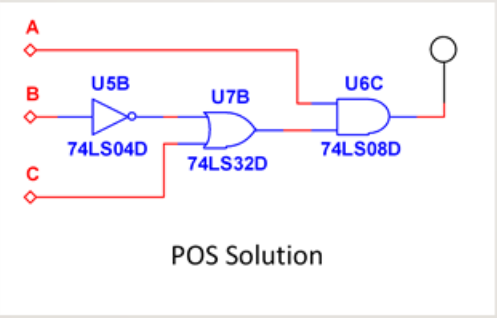


21 LAB 8

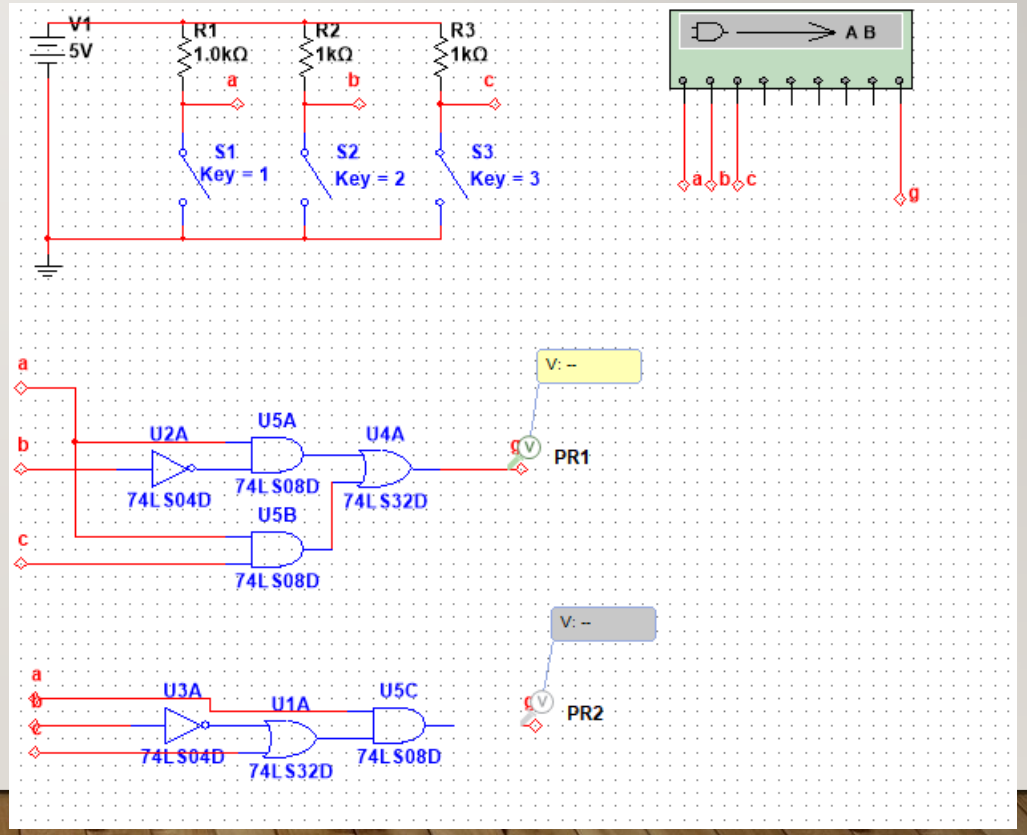
Lab 8 schematic for SOP and POS circuits







Multisim buildup.



22 LAB 8

- Results: We added the lab 7 results into the tables to compare them to the results we got for this lab. If everything was done correctly, they were supposed to match (they did)

Simulated					
				Output	
A	B	C	Lab 7	SOP	POS
0	0	0	0v	0v	0v
0	0	1	0v	0v	0v
0	1	0	0v	0v	0v
0	1	1	0v	0v	0v
1	0	0	5v	5v	5v
1	0	1	5v	5v	5v
1	1	0	0v	0v	0v
1	1	1	5v	5v	5v

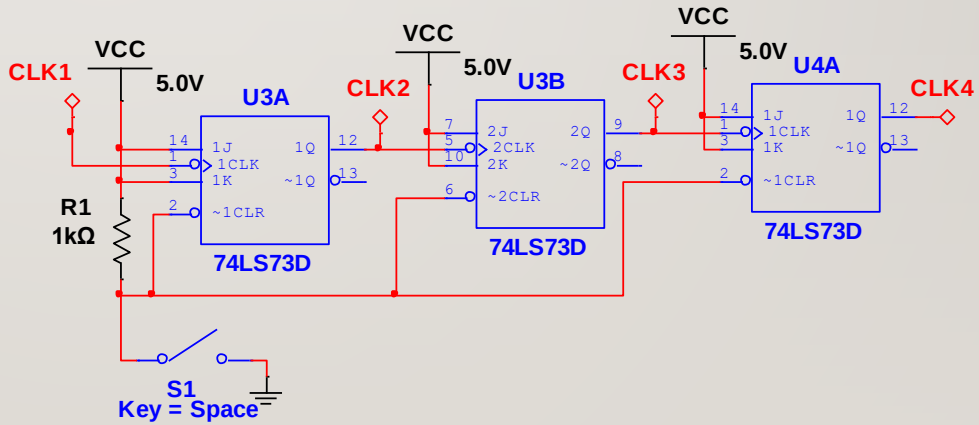
Test					
				Output	
A	B	C	Lab 7	SOP	POS
0	0	0	.1v	0.16v	0.16v
0	0	1	.1v	0.07v	0.16v
0	1	0	.1v	0.07v	0.16v
0	1	1	.1v	0.07v	0.16v
1	0	0	3.9v	4.3v	4.25v
1	0	1	3.9v	4.3v	4.25v
1	1	0	.1v	0.07v	0.16v
1	1	1	3.9v	4.3v	4.25v

23 LAB 8

- Observations: This lab was much easier than Lab 7 as these circuits actually had a designated form (POS and SOP).

24 LAB 9

- Clock lab
- The purpose of this lab is to:
- Many times you can use multiple harmonically related clocks to test a combinational circuits. The Purpose of this lab is to show students how to create a small multiple clock counter circuit that uses JK Flip Flops and a 55 Time

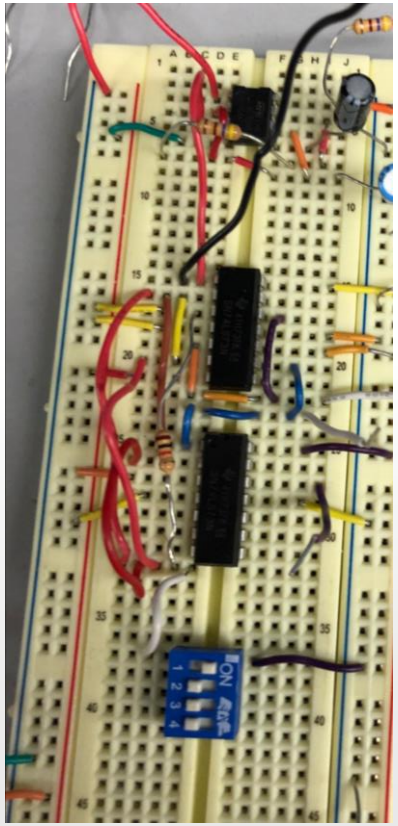


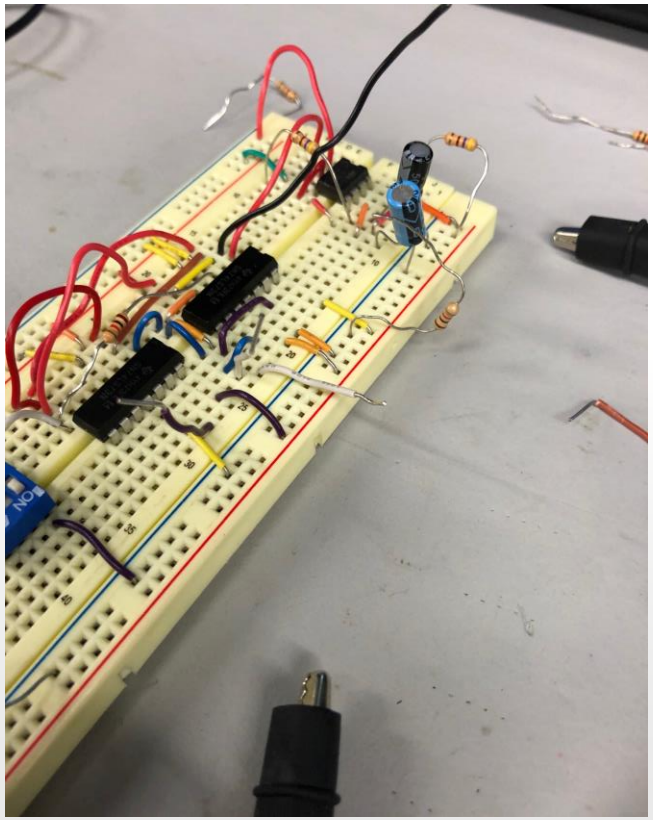
LAB 9

Equipment needed:

- 1 – 555 Timer
- 1 – 1Kohm
- 1 – 4 position dip switch
- 2 – 74LS73 Dual JK flip flop with clear
- 2 – Resistors (To Be Designed)
- 2 – Capacitors (To Be Designed)

LAB 9





LAB 9

- Observations:

Remember to look at data sheets to check layout of parts almost turned on the power with 74ls73 in backwards (I overlooked the little notch being careless) but caught it giving the board one more look at the data sheet and part layout.

THANK YOU FOR A GREAT SEMESTER PROFESSOR BELL!